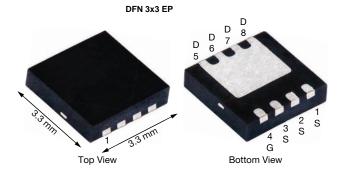


# N-Channel 250 V (D-S) MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	250			
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 10 \text{ V}$	1.5			
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 7.5 \text{ V}$	1.8			
Q <sub>g</sub> typ. (nC)	7.5			
I <sub>D</sub> (A)	2.5			
Configuration	Single			



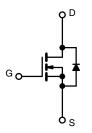
#### **FEATURES**

- Trench power MOSFET
- Low thermal resistance package
- 100 % R<sub>q</sub> and UIS tested



#### **APPLICATIONS**

- Primary side switch
- Synchronous rectification
- DC/DC converter
- Lighting
- Industrial



N-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATING</b>	<b>iS</b> (T <sub>A</sub> = 25 °C, u	inless otherv	vise noted)	
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		$V_{DS}$	250	V
Gate-source voltage		$V_{GS}$	± 20	v
Continuous drain current (T <sub>J</sub> = 150 °C)	T <sub>C</sub> = 25 °C		2.5	
	T <sub>C</sub> = 70 °C		1.8	
	T <sub>A</sub> = 25 °C	l <sub>D</sub>	1.7 <sup>a, b</sup>	
	T <sub>A</sub> = 70 °C		1.3 <sup>a, b</sup>	^
Pulsed drain current (t = 100 μs)		I <sub>DM</sub>	3	A
Continuous source-drain diode current	T <sub>C</sub> = 25 °C		1.5	
	T <sub>A</sub> = 25 °C	T <sub>A</sub> = 25 °C	1.2 <sup>a, b</sup>	
Single pulse avalanche current  L = 0.1 mH		I <sub>AS</sub>	1	
Single pulse avalanche energy	L = 0.1 IIII	E <sub>AS</sub>	1.2	mJ
Maximum power dissipation	T <sub>C</sub> = 25 °C		14.2	
	T <sub>C</sub> = 70 °C		10.8	w
	T <sub>A</sub> = 25 °C	$P_{D}$	2.5 <sup>a, b</sup>	VV
	T <sub>A</sub> = 70 °C	1	1.2 <sup>a, b</sup>	
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Soldering recommendations (peak temperature) a			260	

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient <sup>a</sup>	t ≤ 10 s	$R_{thJA}$	20	25	°C/W	
Maximum junction-to-case (drain)	Steady state	$R_{thJC}$	1.8	2.3	]	

#### Notes

- a. Surface mounted on 1" x 1" FR4 board
- b. t = 10 s
- c. The DFN3x3 package is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- d. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- e. Maximum under steady state conditions is 65 °C/W
- f.  $T_C = 25$  °C



PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static	<u> </u>						
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	250	-	-	V	
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$		-	254	-	1404	
V <sub>GS(th)</sub> temperature coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA	-	-6.9	-	mV/°	
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1	-	3	V	
Gate-source leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	100	nA	
Zero gate voltage drain current		V <sub>DS</sub> = 250 V, V <sub>GS</sub> = 0 V	-	-	1	μΑ	
	I <sub>DSS</sub>	V <sub>DS</sub> = 250 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C	-	-	10		
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	2	-	-	Α	
	_	V <sub>GS</sub> =10 V, I <sub>D</sub> = 0.5 A	-	1.5	-	Ω	
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 7.5 \text{ V}, I_D = 0.5 \text{ A}$	-	1.8	-		
Forward transconductance a	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1.0 A	-	10	-	S	
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>		-	400	-	pF	
Output capacitance	C <sub>oss</sub>	$V_{DS} = 125 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	65	-		
Reverse transfer capacitance	C <sub>rss</sub>	20 / GC /	-	2	-		
		V <sub>DS</sub> = 125 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 21A		10.9	16.5		
Total gate charge	$Q_g$		-	7.5	8.9	nC	
Gate-source charge	Q <sub>qs</sub>	$V_{DS} = 125 \text{ V}, V_{GS} = 7.5 \text{ V}, I_D = 1 \text{ A}$	-	2.7	-		
Gate-drain charge	Q <sub>qd</sub>		-	2.9	-		
Output charge	Q <sub>oss</sub>	V <sub>DS</sub> = 125 V, V <sub>GS</sub> = 0 V	-	30	45		
Gate resistance	$R_g$	f = 1 MHz	0.5	2.3	4.6	Ω	
Turn-on delay time	t <sub>d(on)</sub>		-	8	16		
Rise time	t <sub>r</sub>	$V_{DD} = 125 \text{ V}, R_1 = 41.7 \Omega, I_D \cong 1 \text{ A},$	-	22	35	1	
Turn-off delay time	t <sub>d(off)</sub>	$V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	18	30	1	
Fall time	t <sub>f</sub>		-	22	35	1	
Turn-on delay time	t <sub>d(on)</sub>		-	10	20	ns	
Rise time	t <sub>r</sub>	$V_{DD} = 125 \text{ V}, R_{I} = 41.7 \Omega, I_{D} \cong 1A,$	-	22	40	_	
Turn-off delay time	t <sub>d(off)</sub>	$V_{GEN} = 7.5 \text{ V}, R_g = 1 \Omega$	-	18	30		
Fall time	t <sub>f</sub>		-	25	50	1	
<b>Drain-Source Body Diode Characterist</b>	ics						
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-	-	1.5	Τ.	
Pulse diode forward current	I <sub>SM</sub>	-	-	-	2	A	
Body diode voltage	V <sub>SD</sub>	I <sub>S</sub> = 1.0 A, V <sub>GS</sub> = 0 V	-	0.8	1.2	V	
Body diode reverse recovery time	t <sub>rr</sub>		-	100	150	ns	
Body diode reverse recovery charge	Q <sub>rr</sub>		-	356	550	nC	
Reverse recovery fall time	ta	$I_F = 1.0 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$	-	65	-	ns	
Reverse recovery rise time	t <sub>b</sub>		_	35	_		

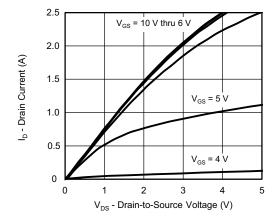
#### Notes

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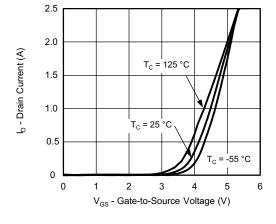
- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

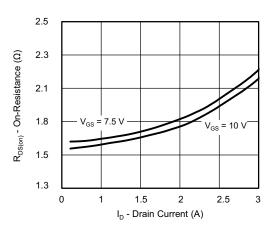




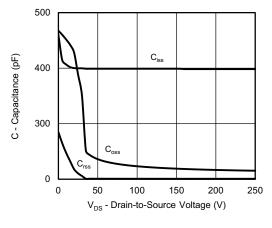
**Output Characteristics** 



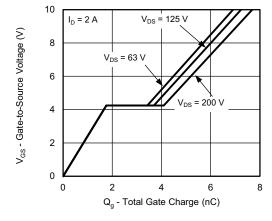
**Transfer Characteristics** 



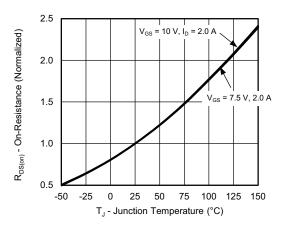
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

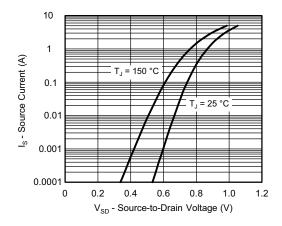


**Gate Charge** 

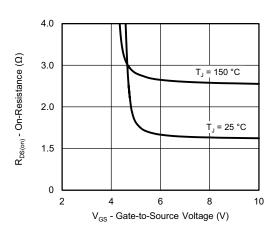


On-Resistance vs. Junction Temperature

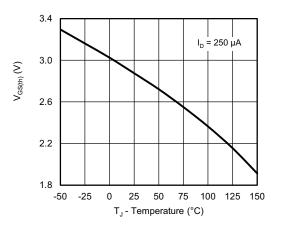




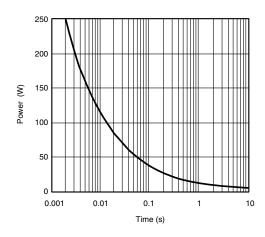
Source-Drain Diode Forward Voltage



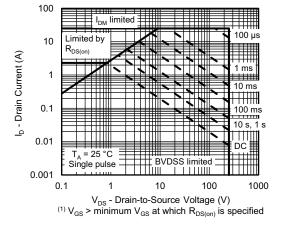
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

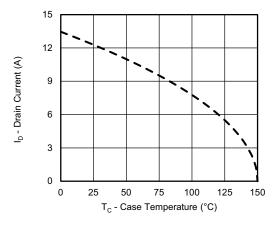


Single Pulse Power, Junction-to-Ambient

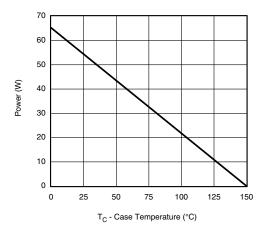


Safe Operating Area, Junction-to-Ambient

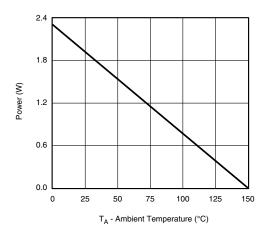




#### Current Derating a



Power, Junction-to-Case

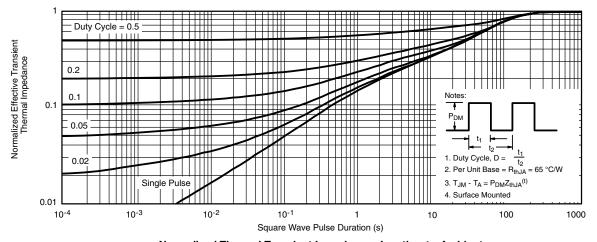


Power, Junction-to-Ambient

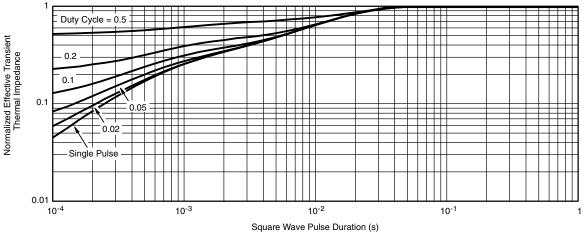
#### Note

a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot



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