

N-Channel 650V (D-S) Power MOSFET

PRODUCT SUMMARY	
V _{DS} (V) at T _J max.	600
R _{DS(on)} at 25 °C (Ω)	V _{GS} = 10 V 0.70
Q _g max. (nC)	43
Q _{gs} (nC)	5
Q _{gd} (nC)	22
Configuration	Single

FEATURES

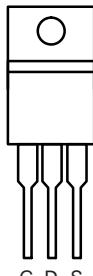
- Low figure-of-merit (FOM) R_{on} × Q_g
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)



APPLICATIONS

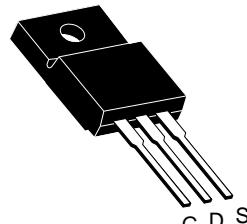
- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial

TO-220AB

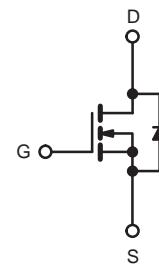


Top View

TO-220 FULLPAK



Top View



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	600	V
Gate-Source Voltage	V _{GS}	± 30	
Continuous Drain Current (T _J = 150 °C)	I _D	12	A
		9.4	
Pulsed Drain Current ^a	I _{DM}	45	
Linear Derating Factor		3.6	W/°C
Single Pulse Avalanche Energy ^b	E _{AS}	9	mJ
Maximum Power Dissipation	P _D	156/34	W
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C
Drain-Source Voltage Slope	dV/dt	15	V/ns
Reverse Diode dV/dt ^d		4.1	
Soldering Recommendations (Peak Temperature) ^c	for 10 s	300	°C

Notes

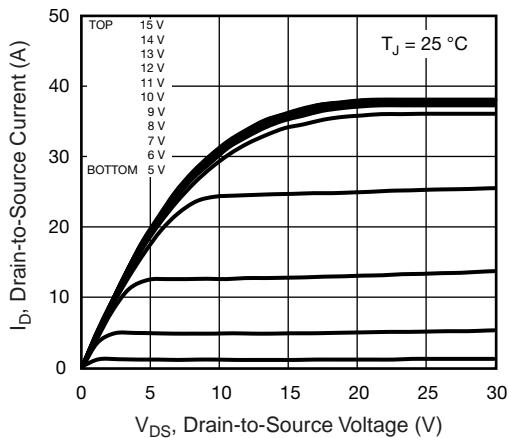
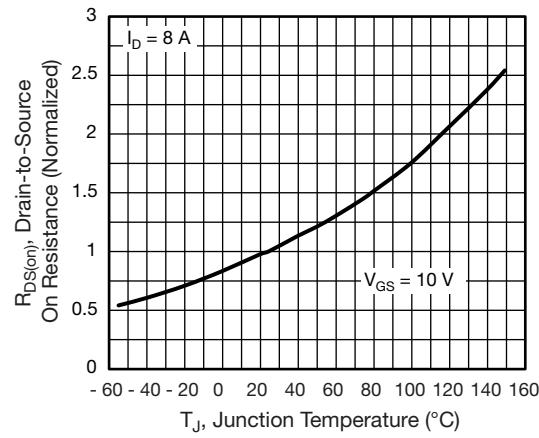
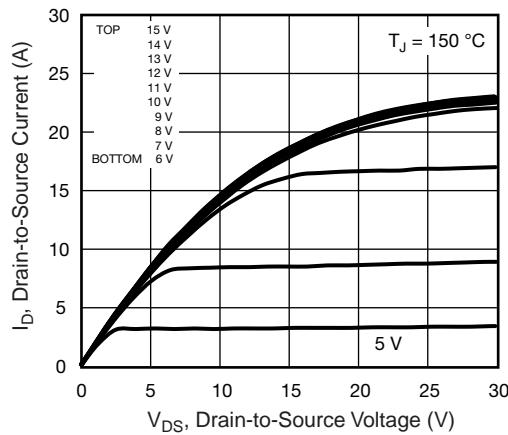
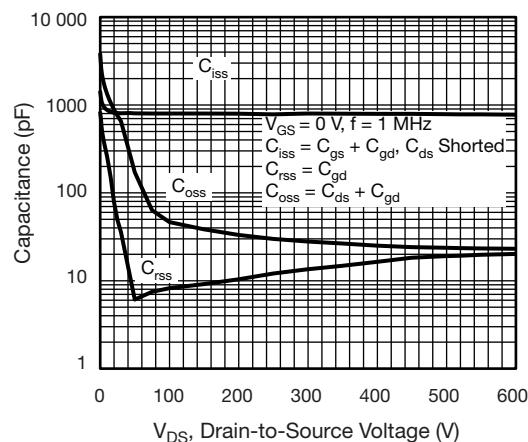
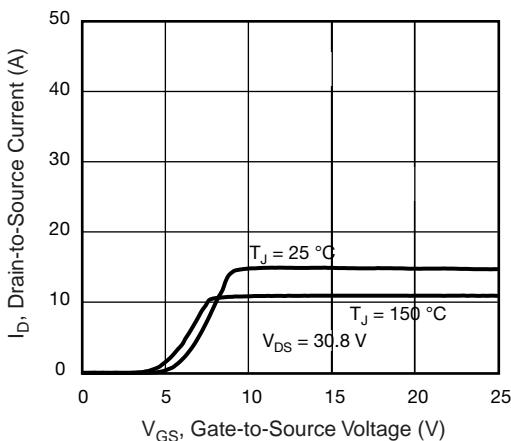
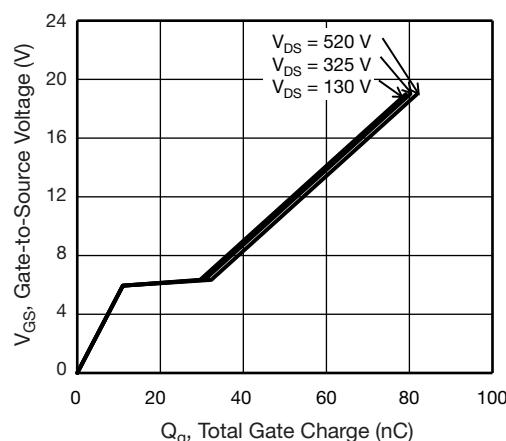
- Repetitive rating; pulse width limited by maximum junction temperature.
- V_{DD} = 50 V, starting T_J = 25 °C, L = 28.2 mH, R_g = 25 Ω, I_{AS} = 4.5 A.
- 1.6 mm from case.
- I_{SD} ≤ I_D, dI/dt = 100 A/μs, starting T_J = 25 °C.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	60	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.8	°C/W

SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)								
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$		600	-	-	V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25°C , $I_D = 1 \text{ mA}$		-	0.75	-	$\text{V}/^\circ\text{C}$	
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$		2	-	4	V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA	
		$V_{GS} = \pm 30 \text{ V}$		-	-	± 1	μA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 650 \text{ V}$, $V_{GS} = 0 \text{ V}$		-	-	1	μA	
		$V_{DS} = 520 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 125^\circ\text{C}$		-	-	10		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$	$I_D = 8 \text{ A}$	-	0.70	-	Ω	
Forward Transconductance	g_{fs}	$V_{DS} = 30 \text{ V}$, $I_D = 8 \text{ A}$		-	16	-	S	
Dynamic								
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$, $V_{DS} = 100 \text{ V}$, $f = 1 \text{ MHz}$		-	800	-	pF	
Output Capacitance	C_{oss}			-	70	-		
Reverse Transfer Capacitance	C_{rss}			-	8	-		
Effective Output Capacitance, Energy Related ^a	$C_{o(er)}$	$V_{DS} = 0 \text{ V}$ to 520 V , $V_{GS} = 0 \text{ V}$		-	63	-		
Effective Output Capacitance, Time Related ^b	$C_{o(tr)}$			-	213	-		
Total Gate Charge	Q_g		$V_{GS} = 10 \text{ V}$	$I_D = 8 \text{ A}$, $V_{DS} = 520 \text{ V}$	-	48	96	nC
Gate-Source Charge	Q_{gs}				-	11	-	
Gate-Drain Charge	Q_{gd}				-	21	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 520 \text{ V}$, $I_D = 8 \text{ A}$, $V_{GS} = 10 \text{ V}$, $R_g = 9.1 \Omega$			-	13	25	ns
Rise Time	t_r				-	11	35	
Turn-Off Delay Time	$t_{d(off)}$				-	81	90	
Fall Time	t_f				-	25	40	
Gate Input Resistance	R_g	$f = 1 \text{ MHz}$, open drain		-	3.5	-	Ω	
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	15	A	
Pulsed Diode Forward Current	I_{SM}			-	-	40		
Diode Forward Voltage	V_{SD}	$T_J = 25^\circ\text{C}$, $I_S = 8 \text{ A}$, $V_{GS} = 0 \text{ V}$		-	-	1.5	V	
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}$, $I_F = I_S = 8 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}$, $V_R = 400 \text{ V}$		-	345	-	ns	
Reverse Recovery Charge	Q_{rr}			-	4.5	-	μC	
Reverse Recovery Current	I_{RRM}			-	35	-	A	

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

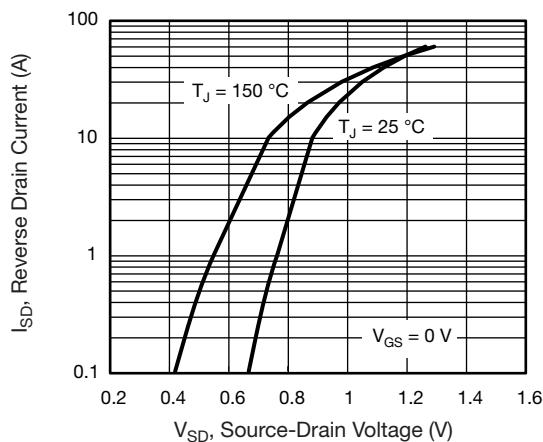


Fig. 7 - Typical Source-Drain Diode Forward Voltage

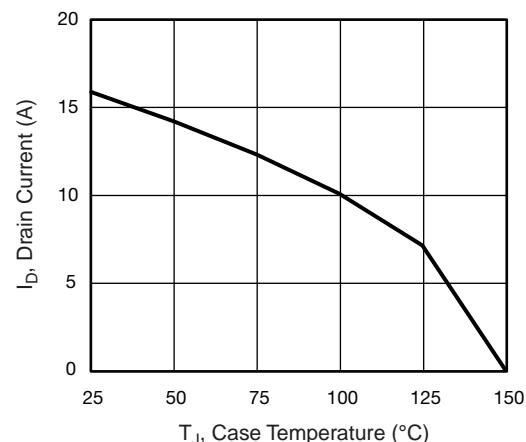


Fig. 9 - Maximum Drain Current vs. Case Temperature

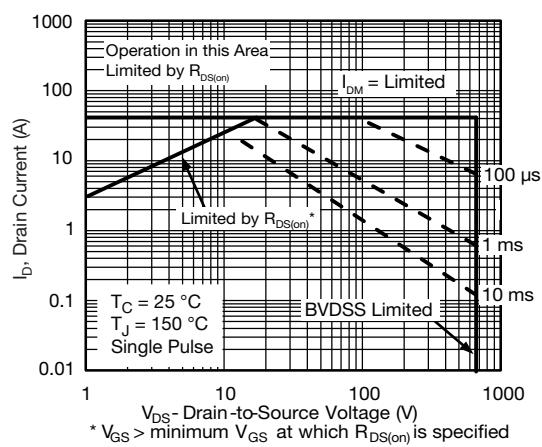


Fig. 8 - Maximum Safe Operating Area

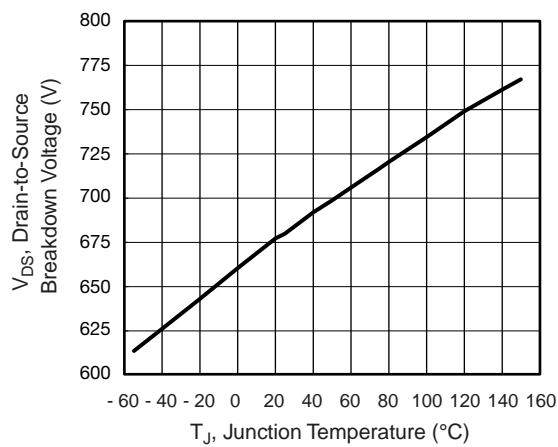


Fig. 10 - Temperature vs. Drain-to-Source Voltage

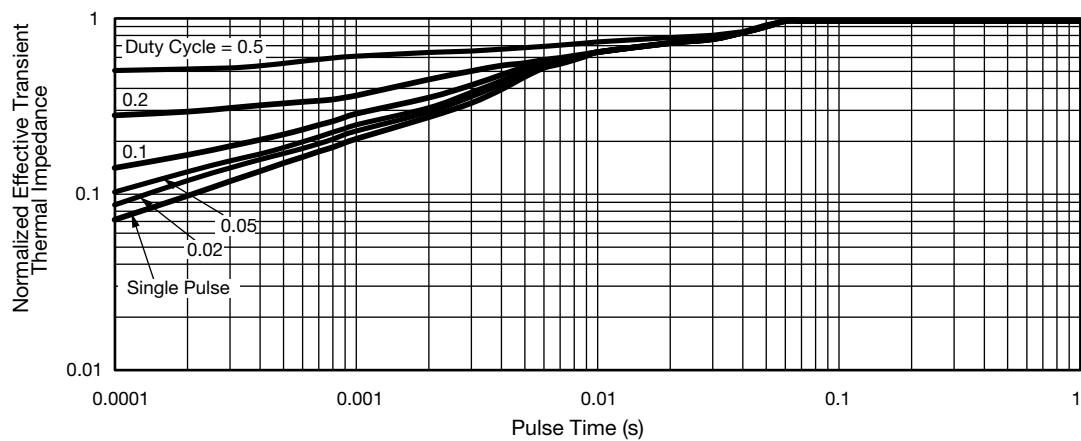


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

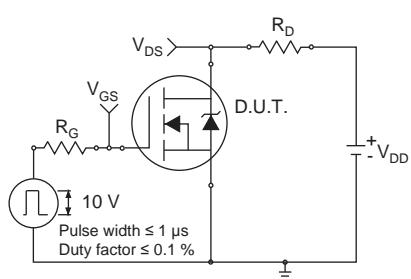


Fig. 12 - Switching Time Test Circuit

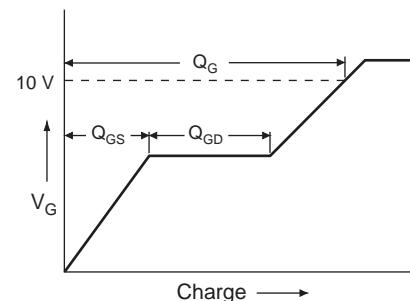


Fig. 16 - Basic Gate Charge Waveform

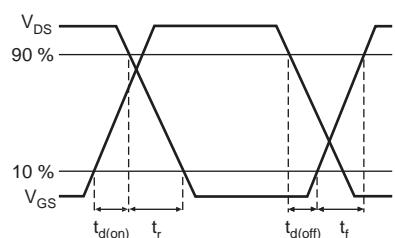


Fig. 13 - Switching Time Waveforms

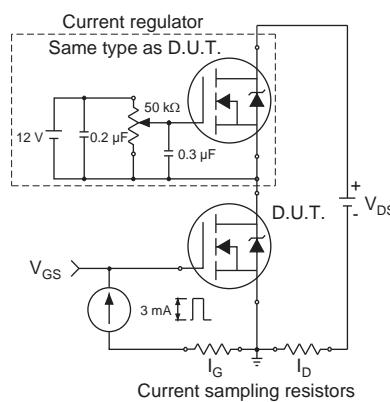


Fig. 17 - Gate Charge Test Circuit

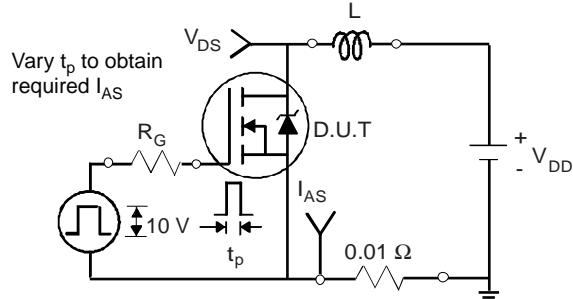


Fig. 14 - Unclamped Inductive Test Circuit

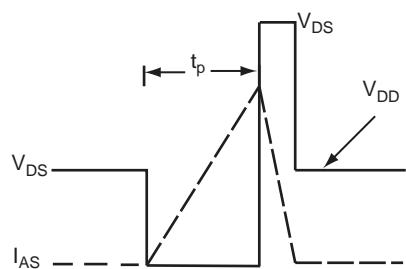
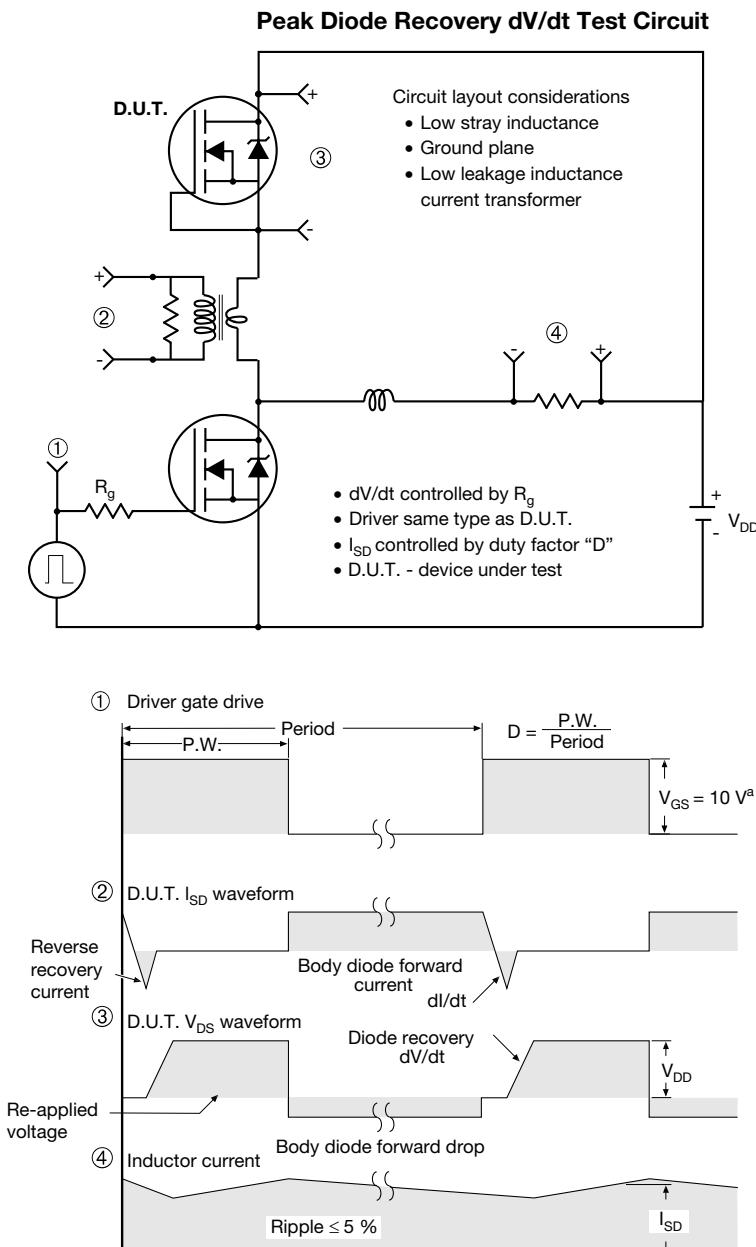
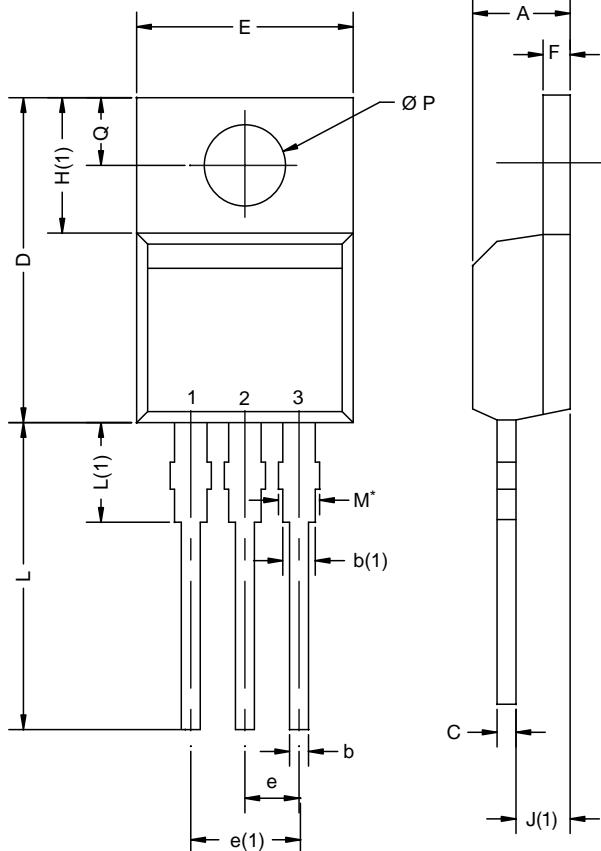


Fig. 15 - Unclamped Inductive Waveforms

**Fig. 18 - For N-Channel**

TO-220AB

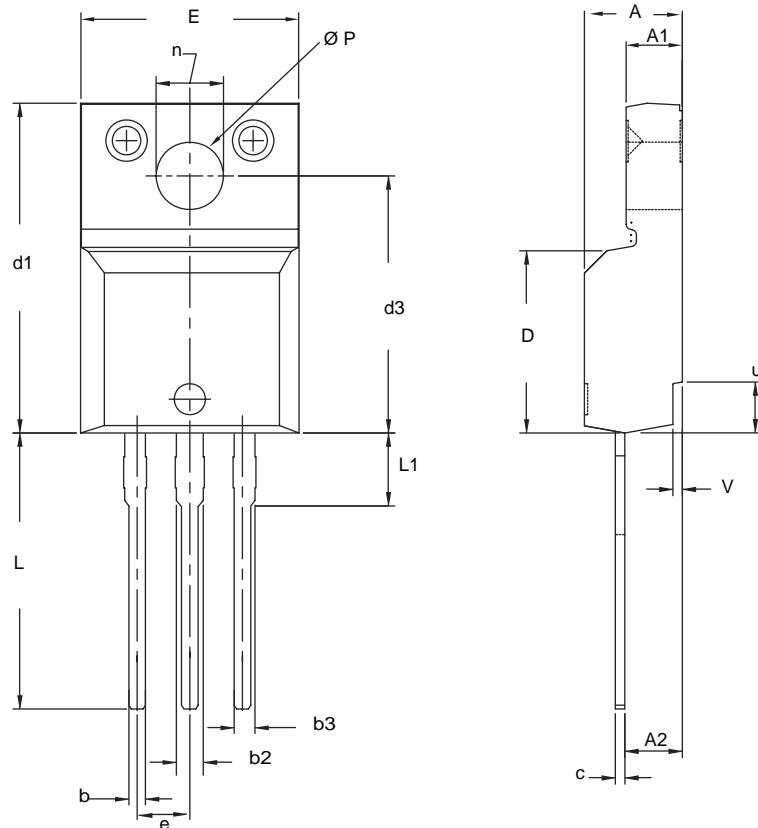


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
Ø P	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

ECN: X12-0208-Rev. N, 08-Oct-12
DWG: 5471

Notes

* M = 1.32 mm to 1.62 mm (dimension including protrusion)
Heatsink hole for HVM

TO-220 FULLPAK (HIGH VOLTAGE)

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
ØP	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
v	0.400	0.500	0.016	0.020

ECN: X09-0126-Rev. B, 26-Oct-09
DWG: 5972

Notes

1. To be used only for process drawing.
2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
3. All critical dimensions should C meet $C_{pk} > 1.33$.
4. All dimensions include burrs and plating thickness.
5. No chipping or package damage.

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