

## N-Channel 650V (D-S) Super Junction Power MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V) at $T_J$ max.	650	
$R_{DS(on)}$ at 25 °C ( $\Omega$ )	$V_{GS} = 10\text{ V}$	0.50
$Q_g$ max. (nC)	25	
$Q_{gs}$ (nC)	2.0	
$Q_{gd}$ (nC)	2.7	
Configuration	Single	

### FEATURES

- Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low input capacitance ( $C_{iss}$ )
- Reduced switching and conduction losses
- Ultra low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)

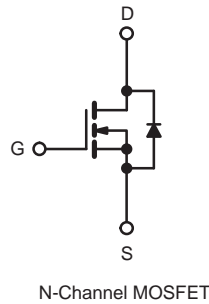
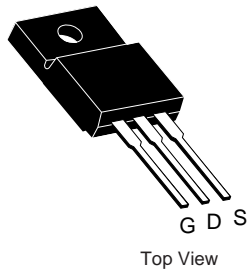


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### APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial

TO-220 FULLPAK



### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ °C}$ , unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V <sub>DS</sub>	650	V
Gate-Source Voltage			V <sub>GS</sub>	± 30	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	I <sub>D</sub>	9	A
		T <sub>C</sub> = 100 °C		6	
Pulsed Drain Current <sup>a</sup>			I <sub>DM</sub>	21	
Linear Derating Factor				1.5	W/°C
Single Pulse Avalanche Energy <sup>b</sup>			E <sub>AS</sub>	86	mJ
Maximum Power Dissipation			P <sub>D</sub>	83	W
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Drain-Source Voltage Slope	T <sub>J</sub> = 125 °C		dV/dt	50	V/ns
Reverse Diode dV/dt <sup>d</sup>		4.5			
Soldering Recommendations (Peak Temperature) <sup>c</sup>	for 10 s			300	°C


#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50\text{ V}$ , starting  $T_J = 25\text{ °C}$ ,  $L = 28.2\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 3.5\text{ A}$ .
- 1.6 mm from case.
- $I_{SD} \leq I_D$ ,  $dI/dt = 100\text{ A}/\mu\text{s}$ , starting  $T_J = 25\text{ °C}$ .

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	63	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.6	

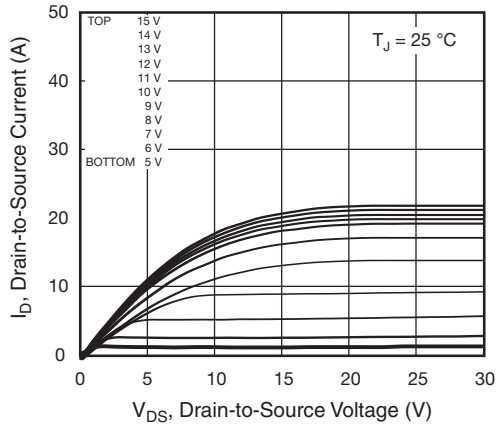
**SPECIFICATIONS** ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		650	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.65	-	V/°C
Gate-Source Threshold Voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2	-	4	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
		V <sub>GS</sub> = ± 30 V		-	-	± 1	μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V		-	-	1	μA
		V <sub>DS</sub> = 520 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	10	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 4 A	-	0.50	-	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 4 A		-	16	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 100 V, f = 1 MHz		-	360	-	pF
Output Capacitance	C <sub>oss</sub>			-	25	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	12	-	
Effective Output Capacitance, Energy Related <sup>a</sup>	C <sub>o(er)</sub>	V <sub>DS</sub> = 0 V to 520 V, V <sub>GS</sub> = 0 V		-	45	-	pF
Effective Output Capacitance, Time Related <sup>b</sup>	C <sub>o(tr)</sub>			-	62	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 4 A, V <sub>DS</sub> = 520 V	-	25	-	nC
Gate-Source Charge	Q <sub>gs</sub>			-	2.0	-	
Gate-Drain Charge	Q <sub>gd</sub>			-	2.7	-	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 520 V, I <sub>D</sub> = 4 A, V <sub>GS</sub> = 10 V, R <sub>g</sub> = 9.1 Ω		-	25	-	ns
Rise Time	t <sub>r</sub>			-	55	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	70	-	
Fall Time	t <sub>f</sub>			-	40	-	
Gate Input Resistance	R <sub>g</sub>	f = 1 MHz, open drain		-	3.5	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	7	A
Pulsed Diode Forward Current	I <sub>SM</sub>			-	-	18	
Diode Forward Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 4 A, V <sub>GS</sub> = 0 V		-	-	1.5	V
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = I <sub>S</sub> = 4 A, dI/dt = 100 A/μs, V <sub>R</sub> = 400 V		-	190	-	ns
Reverse Recovery Charge	Q <sub>rr</sub>			-	2.3	-	μC
Reverse Recovery Current	I <sub>RRM</sub>			-	10	-	A

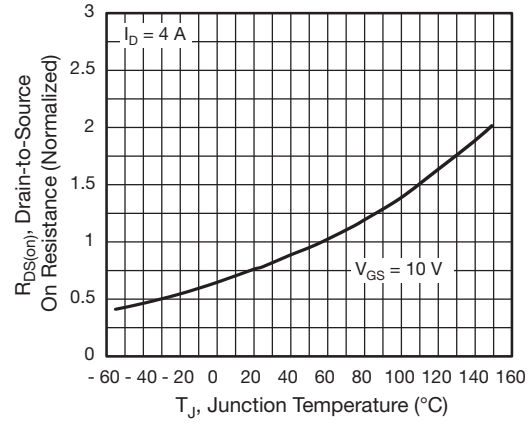
**Notes**

- a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .  
 b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .

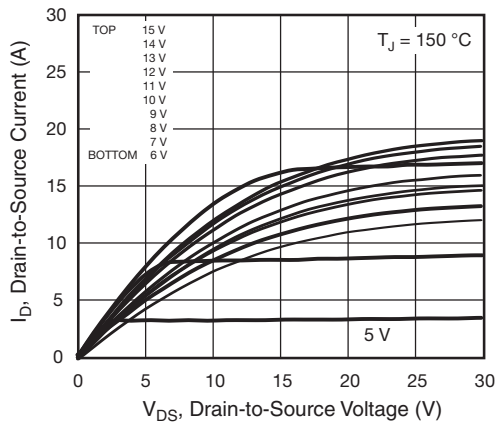
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



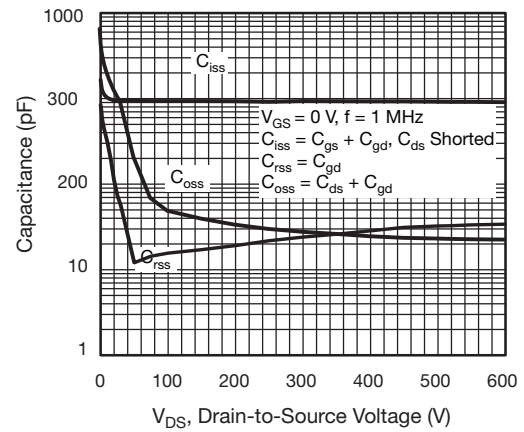
**Fig. 1 - Typical Output Characteristics**



**Fig. 4 - Normalized On-Resistance vs. Temperature**



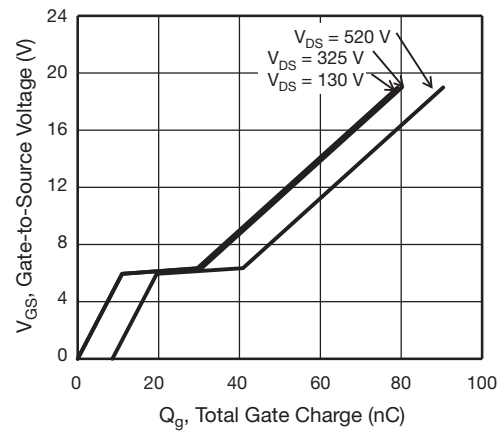
**Fig. 2 - Typical Output Characteristics**



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**

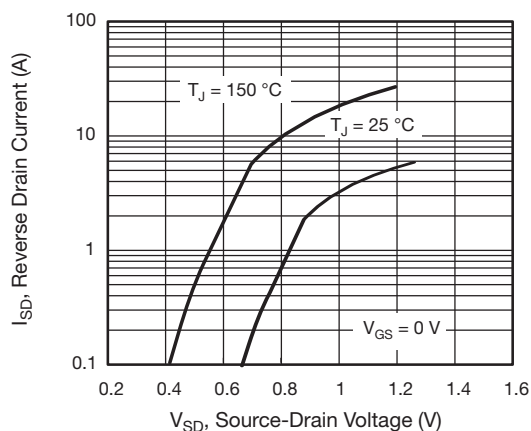


Fig. 7 - Typical Source-Drain Diode Forward Voltage



Fig. 9 - Maximum Drain Current vs. Case Temperature

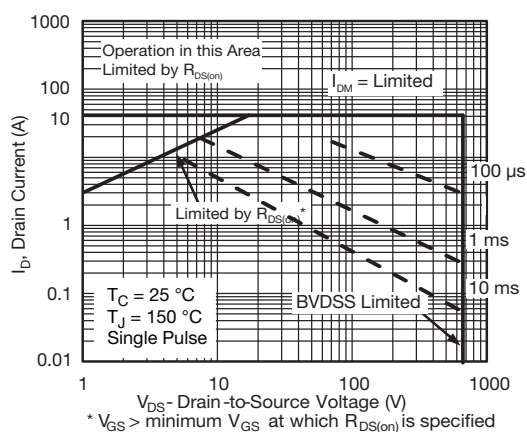


Fig. 8 - Maximum Safe Operating Area

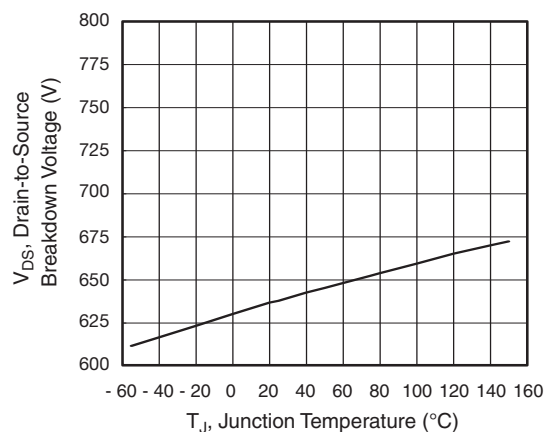


Fig. 10 - Temperature vs. Drain-to-Source Voltage

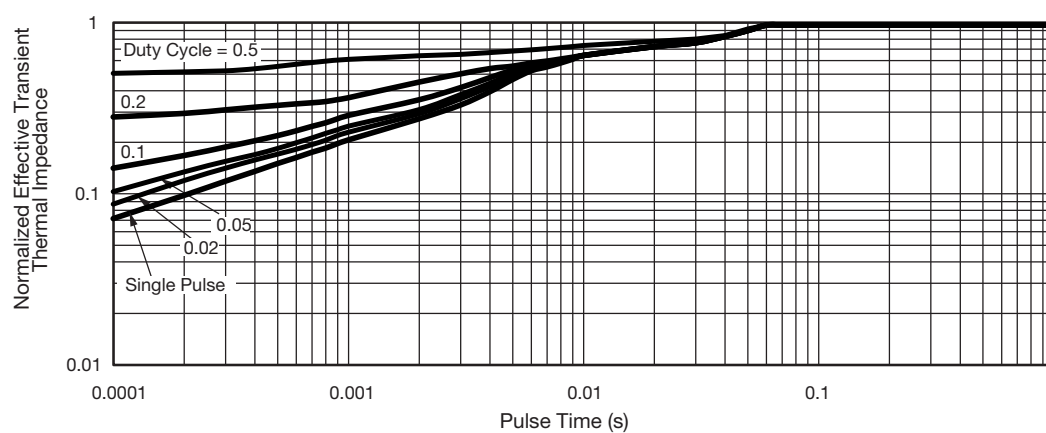


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

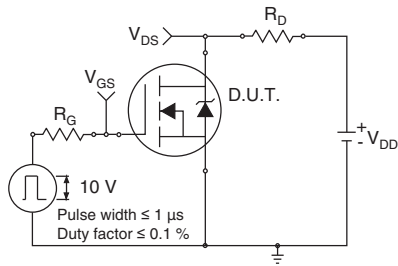


Fig. 12 - Switching Time Test Circuit

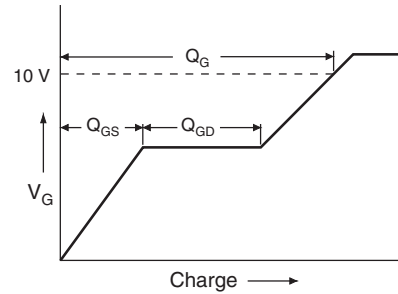


Fig. 16 - Basic Gate Charge Waveform

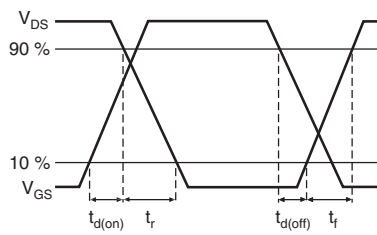


Fig. 13 - Switching Time Waveforms

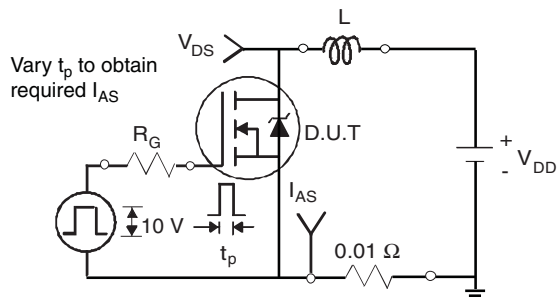


Fig. 14 - Unclamped Inductive Test Circuit

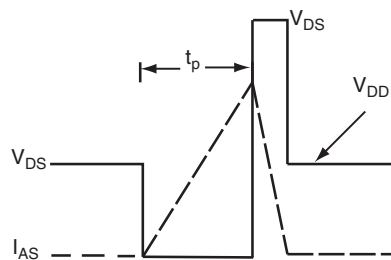


Fig. 15 - Unclamped Inductive Waveforms

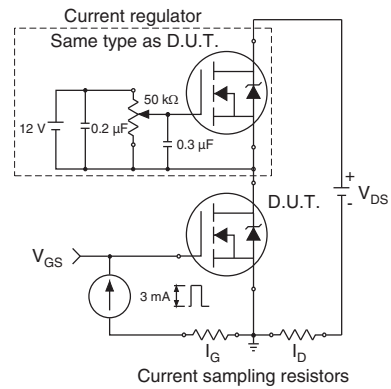
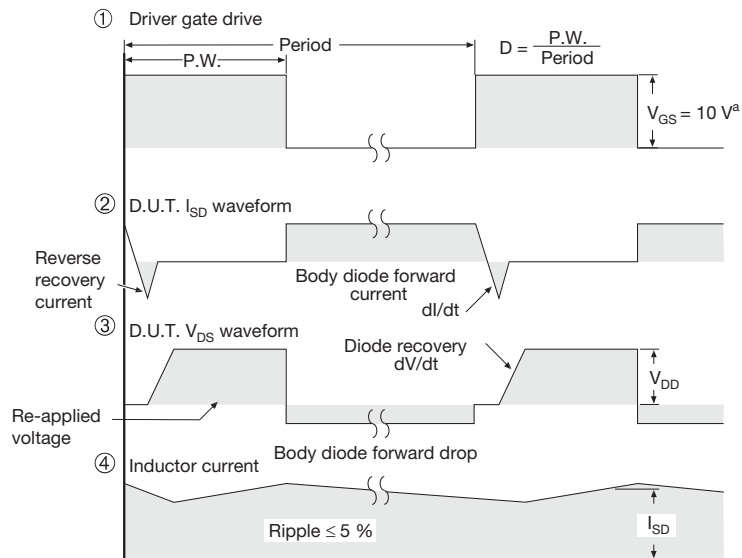
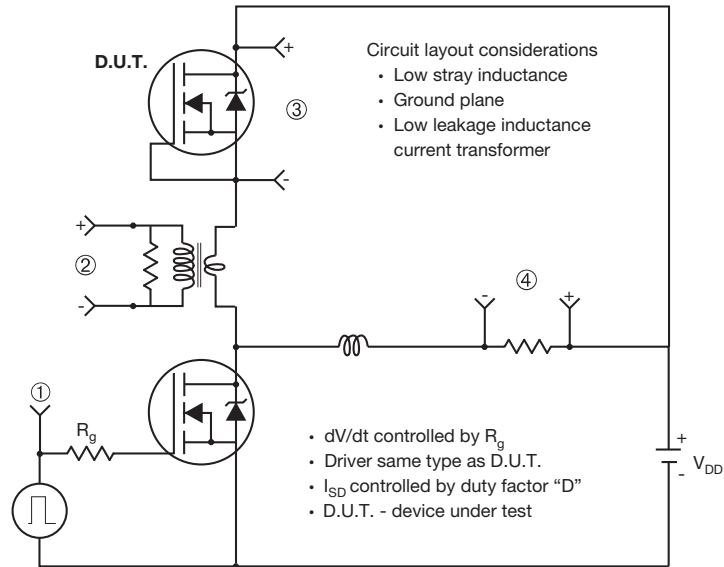


Fig. 17 - Gate Charge Test Circuit

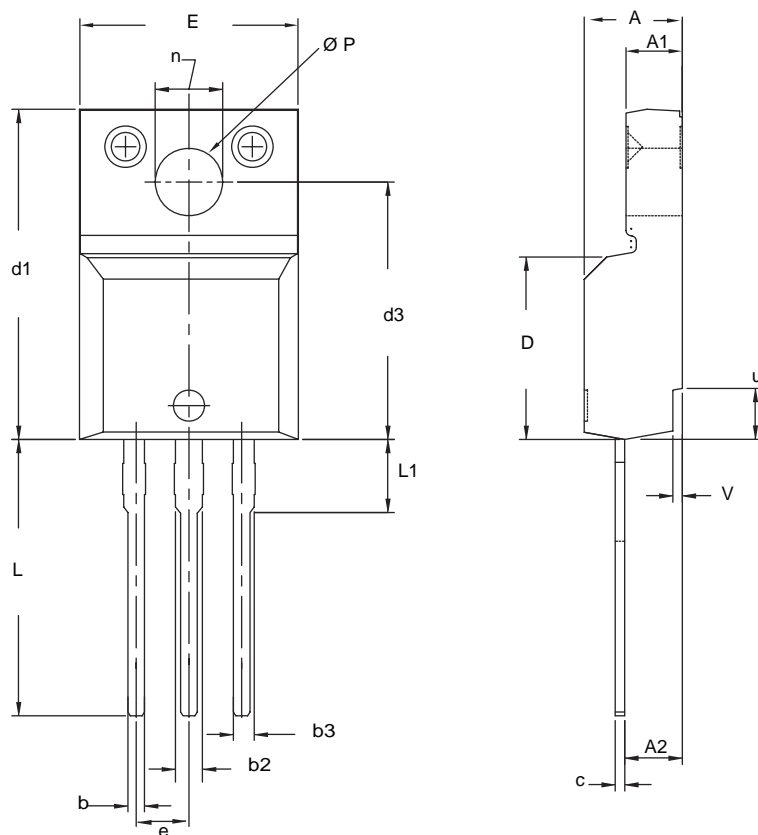
### Peak Diode Recovery $dV/dt$ Test Circuit



**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 18 - For N-Channel**

**TO-220 FULLPAK (HIGH VOLTAGE)**

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
v	0.400	0.500	0.016	0.020

ECN: X09-0126-Rev. B, 26-Oct-09  
DWG: 5972

**Notes**

1. To be used only for process drawing.
2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
3. All critical dimensions should C meet  $C_{pk} > 1.33$ .
4. All dimensions include burrs and plating thickness.
5. No chipping or package damage.

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