

N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY								
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)					
<u></u>	0.076 at V _{GS} = 10 V	5.5	29 nC					
60	0.088 at V _{GS} = 4.5 V	4.5	29110					

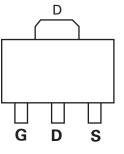
FEATURES

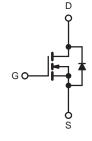
- Halogen-free
- Trench Power MOSFET

APPLICATIONS

· Load Switches for Portable Devices







N-Channel MOSFET

ABSOLUTE MAXIMUM RATIN	IGS T _A = 25 °C,	unless otherwi	se noted		
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage		V _{DS}	60	V	
Gate-Source Voltage	V _{GS}	± 20	V		
	T _C = 25 °C		5.5 ^a		
Continuous Drain Current ($T_1 = 150$ °C)	T _C = 70 °C		4 ^a		
	T _A = 25 °C	I _D	4.7 ^{a, b, c}		
	T _A = 70 °C	1	4 ^{a, b, c}	A	
Pulsed Drain Current	I _{DM}	20			
Continuous Source-Drain Diode Current	T _C = 25 °C	I _S	5.2		
Continuous Source-Drain Diode Current	T _A = 25 °C	'5	5.1 ^{b, c}		
	T _C = 25 °C		5.3		
Maximum Power Dissipation	T _C = 70 °C	P _D	4	w	
	T _A = 25 °C		2.5 ^{b, c}	vv	
	T _A = 70 °C	1	1.6 ^{b, c}		
Operating Junction and Storage Temperatur	T _J , T _{stg}	- 55 to 150	°C		
Soldering Recommendations (Peak Temperation	ature) ^{e, f}		260	U U	

THERMAL RESISTANCE BATINGS

Parameter	Symbol Typical		Maximum	Unit					
Maximum Junction-to-Ambient ^{a, c, d}	t ≤ 5 s	R _{thJA}	40	50	°C/W				
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	15	20	0/11				

Notes:

a. Package limited, T_C = 25 °C.
b. Surface Mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. Maximum under Steady State conditions is 95 °C/W.

e. See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

f. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS $T_J = 25 \ ^{\circ}C$,	unless othe	erwise noted				
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 V, I_{D} = 250 \mu A$	60			V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250 μA		25		
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)} / T_J$	iD = 200 μΛ		- 4.0		mV/°C
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	1.5		3.0	V
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 12 V$			± 100	nA
Zara Cata Valtaga Drain Current	1	$V_{DS} = 60 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			1	μA
Zero Gate Voltage Drain Current	IDSS	V_{DS} = 60 V, V_{GS} = 0 V, T_{J} = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \geq 5$ V, V_{GS} = 4.5 V	25			А
	D	$V_{GS} = 4.5 \text{ V}, I_{D} = 3.3 \text{ A}$		0.088		
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 4.5 \text{ A}$		0.076		Ω
Forward Transconductance ^a	9 _{fs}	V _{DS} = 10 V, I _D = 4.3 A		45		S
Dynamic ^b						
Input Capacitance	C _{iss}			800		
Output Capacitance	C _{oss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz		120		pF
Reverse Transfer Capacitance	C _{rss}			100		1
Total Qata Obarra	0	$V_{DS} = 10 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 6.3 \text{ A}$		22	33	nC
Total Gate Charge	Qg			10	15	
Gate-Source Charge	Q _{gs}	V_{DS} = 10 V, V_{GS} = 4.5 V, I_{D} = 6.3 A		2.5		
Gate-Drain Charge	Q _{gd}			1.7		
Gate Resistance	Rg	f = 1 MHz		2.4		Ω
Turn-on Delay Time	t _{d(on)}			15	25	
Rise Time	t _r	V_{DD} = 10 V, R_L = 1.5 Ω		10	15	-
Turn-Off Delay Time	t _{d(off)}	$\text{I}_\text{D}\cong$ 6.7 A, V_GEN = 4.5 V, R_g = 1 Ω		35	55	
Fall Time	t _f	f		12	20	1
Turn-on Delay Time	t _{d(on)}			10	15	ns
Rise Time	t _r	V_{DD} = 10 V, R _L = 1.5 Ω		12	20	-
Turn-Off Delay Time	t _{d(off)}	$\text{I}_\text{D}\cong\text{6.7}$ A, V_GEN = 10 V, R_g = 1 Ω		25	40	
Fall Time	t _f			10	15	-
Drain-Source Body Diode Characteristi	cs					
Continuous Source-Drain Diode Current	ا _S	T _C = 25 °C			7.2	A
Pulse Diode Forward Current	I _{SM}				25	A
Body Diode Voltage	V _{SD}	$I_{S} = 6.7 \text{ A}, V_{GS} = 0 \text{ V}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}			20	40	ns
Body Diode Reverse Recovery Charge	Q _{rr}			10	20	nC
Reverse Recovery Fall Time	ta	$I_F = 6.7 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 \text{ °C}$		10		
Reverse Recovery Rise Time	t _b			10		ns

Notes:

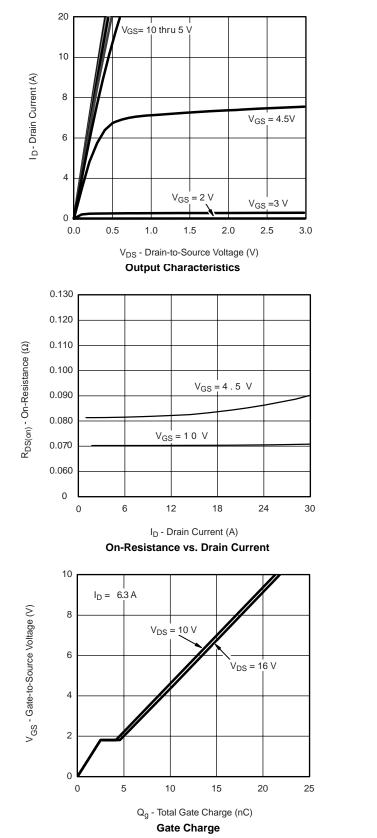
a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %

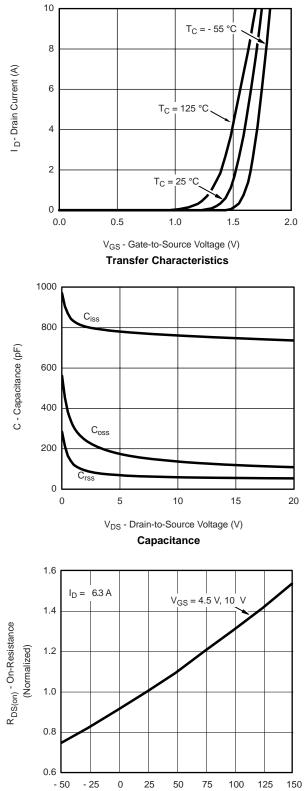
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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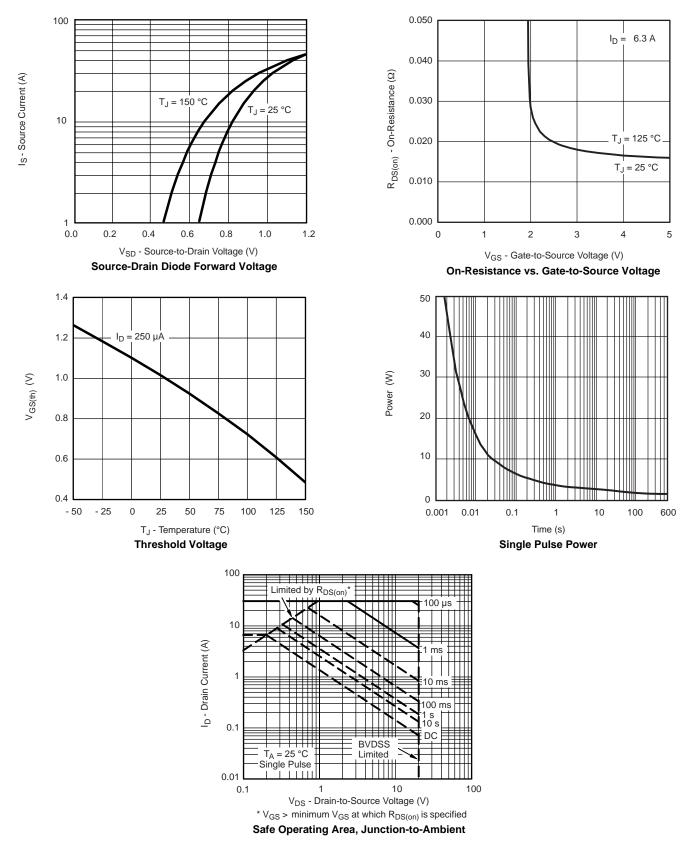




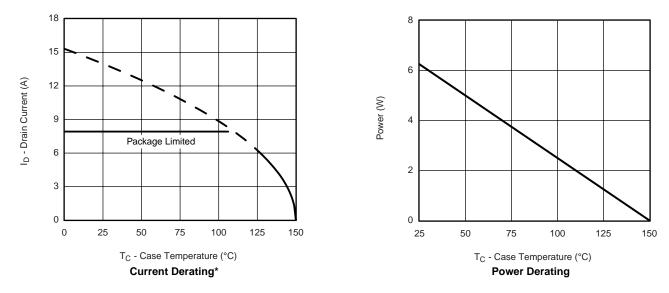
 T_J - Junction Temperature (°C)

On-Resistance vs. Junction Temperature



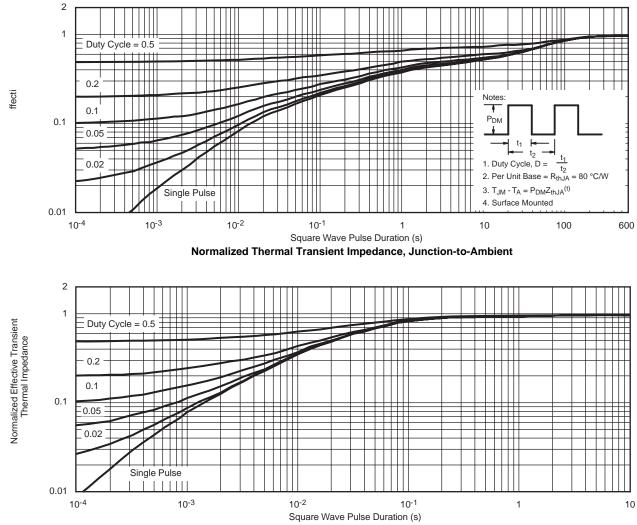






* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



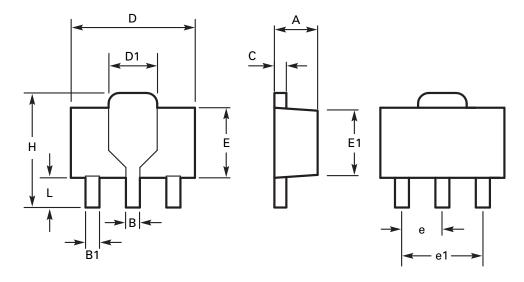


Normalized Thermal Transient Impedance, Junction-to-Foot

VBI1695



Package outline - SOT89



DIM	Millim	neters	Inc	Inches DIM Millimeters Inche		Millimeters		hes	
	Min	Max	Min	Max		Min	Max	Min	Max
Α	1.40	1.60	0.550	0.630	E	2.29	2.60	0.090	0.102
В	0.44	0.56	0.017	0.022	E1	2.13	2.29	0.084	0.090
B1	0.36	0.48	0.014	0.019	е	1.50 BSC		0.059 BSC	
С	0.35	0.44	0.014	0.017	e1	3.00 BSC		0.118 BSC	
D	4.40	4.60	0.173	0.181	Н	3.94	4.25	0.155	0.167
D1	1.62	1.83	0.064	0.072	L	0.89	1.20	0.035	0.047

Note: Controlling dimensions are in millimeters. Approximate dimensions are provided in inches



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