

## Power MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	750	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	6.5
$Q_g$ (Max.) (nC)	38	
$Q_{gs}$ (nC)	5.0	
$Q_{gd}$ (nC)	21	
Configuration	Single	

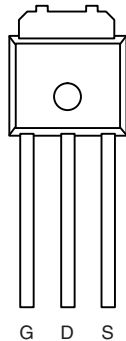
### FEATURES

- Dynamic  $dV/dt$  Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC



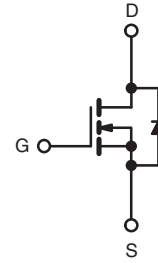
Available  
**RoHS\***  
 COMPLIANT

TO-251



Top View

Drain Connected to  
 Drain-Tab



N-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V <sub>DS</sub>	750	V
Gate-Source Voltage			V <sub>GS</sub>	± 20	
Continuous Drain Current	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	I <sub>D</sub>	1.8	A
		T <sub>C</sub> = 100 °C		1.2	
Pulsed Drain Current <sup>a</sup>			I <sub>DM</sub>	7.2	
Linear Derating Factor				0.43	W/°C
Single Pulse Avalanche Energy <sup>b</sup>			E <sub>AS</sub>	180	mJ
Repetitive Avalanche Current <sup>a</sup>			I <sub>AR</sub>	1.8	A
Repetitive Avalanche Energy <sup>a</sup>			E <sub>AR</sub>	5.4	mJ
Maximum Power Dissipation	T <sub>C</sub> = 25 °C		P <sub>D</sub>	54	W
Peak Diode Recovery dV/dt <sup>c</sup>			dV/dt	2.0	V/ns
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

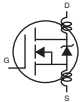

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 104\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 1.8\text{ A}$  (see fig. 12).
- $I_{SD} \leq 1.8\text{ A}$ ,  $dI/dt \leq 80\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq 600$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.50	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	2.3	

**SPECIFICATIONS** ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$		750	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$		-	0.98	-	$\text{V}/^\circ\text{C}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 800\text{ V}$ , $V_{GS} = 0\text{ V}$		-	-	100	$\mu\text{A}$
		$V_{DS} = 640\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ }^\circ\text{C}$		-	-	500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 1.1\text{ A}^b$	-	6.5	-	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 100\text{ V}$ , $I_D = 1.1\text{ A}^b$		0.80	-	-	S
Dynamic							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 25\text{ V}$ , $f = 1.0\text{ MHz}$ , see fig. 5		-	530	-	pF
Output Capacitance	$C_{oss}$			-	150	-	
Reverse Transfer Capacitance	$C_{rss}$			-	90	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 1.8\text{ A}$ , $V_{DS} = 400\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	38	nC
Gate-Source Charge	$Q_{gs}$			-	-	5.0	
Gate-Drain Charge	$Q_{gd}$			-	-	21	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 400\text{ V}$ , $I_D = 1.8\text{ A}$ , $R_g = 18\text{ }\Omega$ , $R_D = 230\text{ }\Omega$ , see fig. 10 <sup>b</sup>		-	8.2	-	ns
Rise Time	$t_r$			-	17	-	
Turn-Off Delay Time	$t_{d(off)}$			-	58	-	
Fall Time	$t_f$			-	27	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	$L_S$			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	1.8	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	7.2	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_S = 1.8\text{ A}$ , $V_{GS} = 0\text{ V}^b$		-	-	1.4	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_F = 1.8\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}^b$		-	380	570	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	0.94	1.4	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
 b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

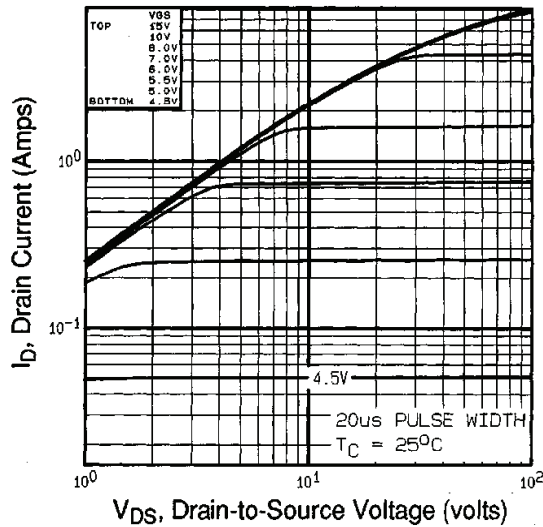
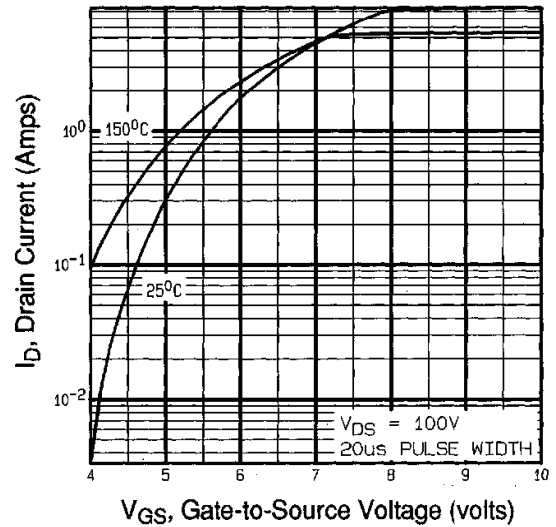
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)
Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^{\circ}\text{C}$ 

Fig. 3 - Typical Transfer Characteristics

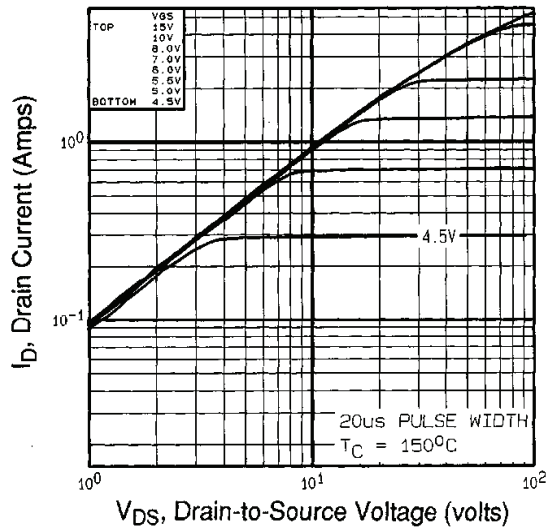
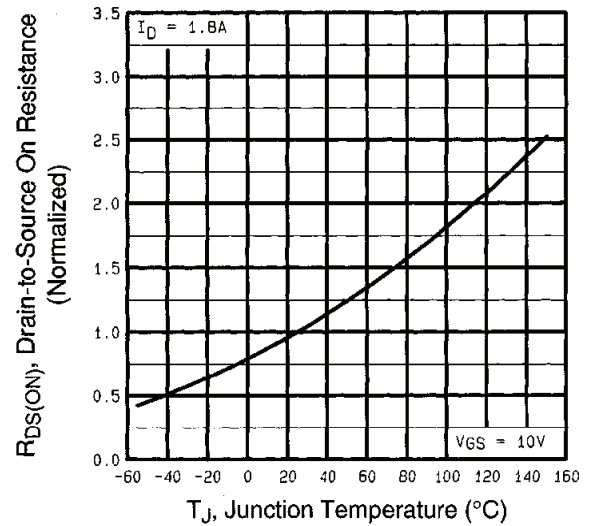
Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^{\circ}\text{C}$ 

Fig. 4 - Normalized On-Resistance vs. Temperature

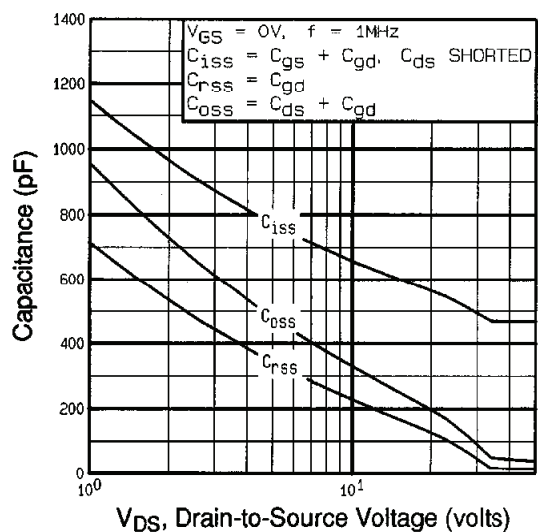


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

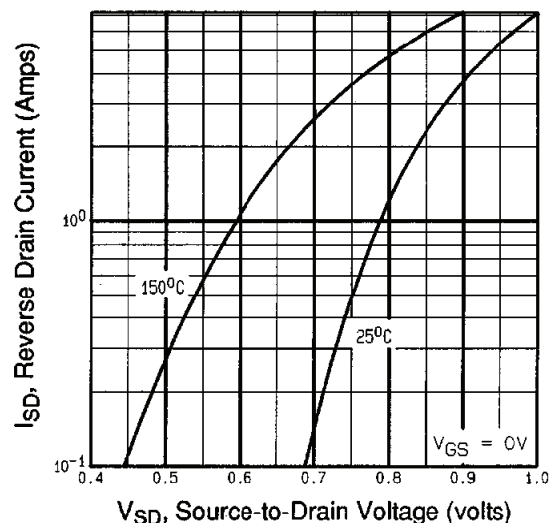


Fig. 7 - Typical Source-Drain Diode Forward Voltage

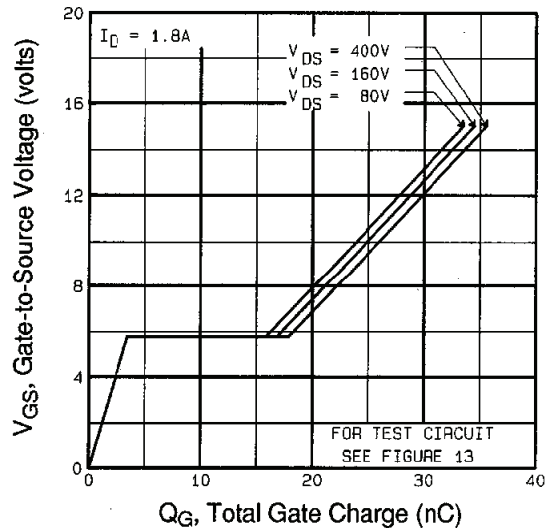


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

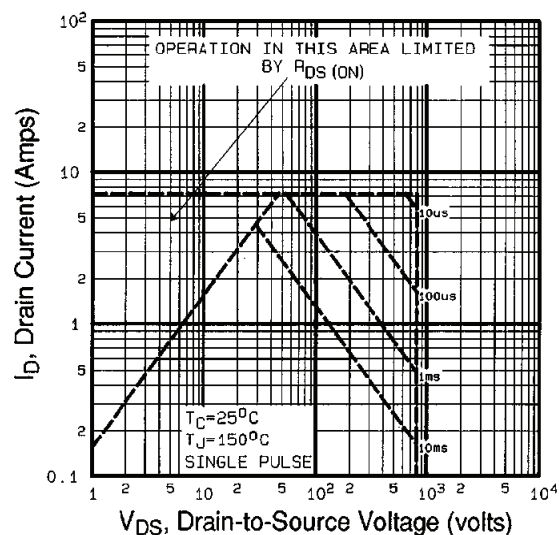


Fig. 8 - Maximum Safe Operating Area

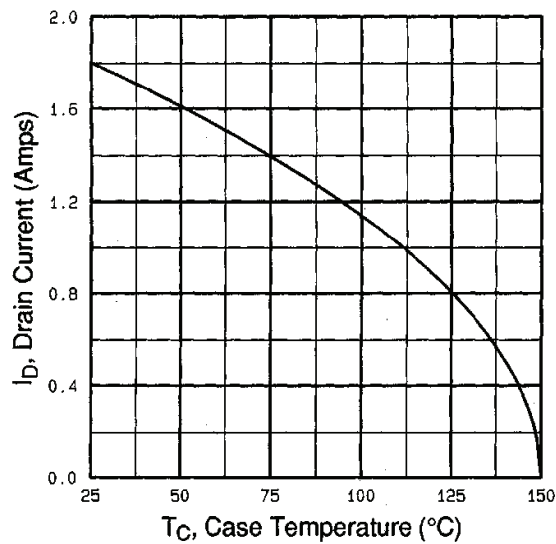


Fig. 9 - Maximum Drain Current vs. Case Temperature

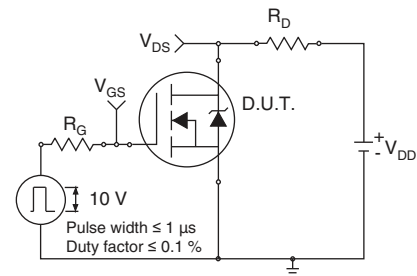


Fig. 10a - Switching Time Test Circuit

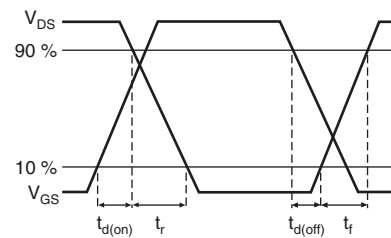


Fig. 10b - Switching Time Waveforms

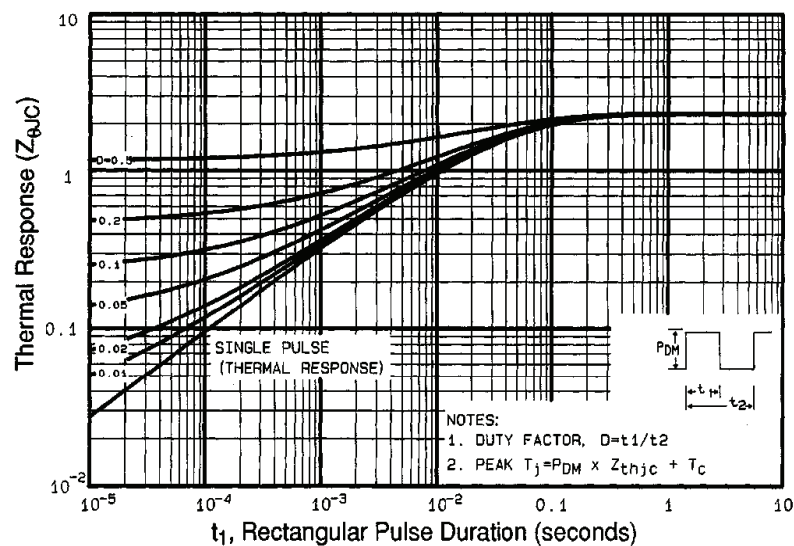


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

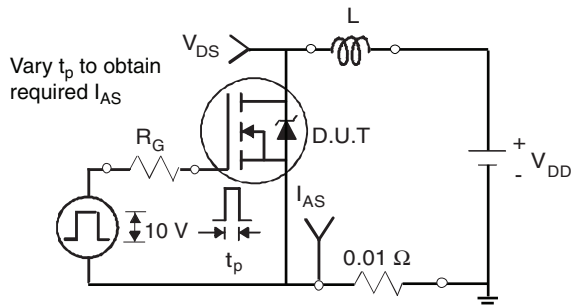


Fig. 12a - Unclamped Inductive Test Circuit

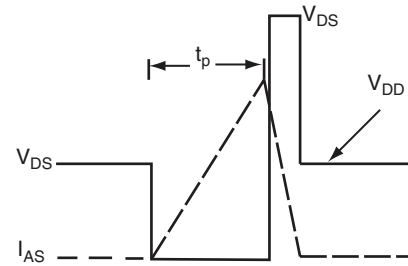


Fig. 12b - Unclamped Inductive Waveforms

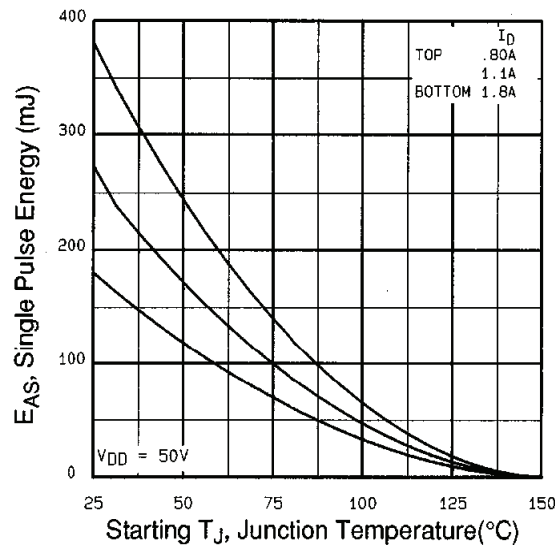


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

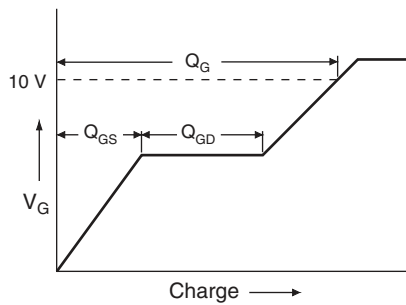


Fig. 13a - Basic Gate Charge Waveform

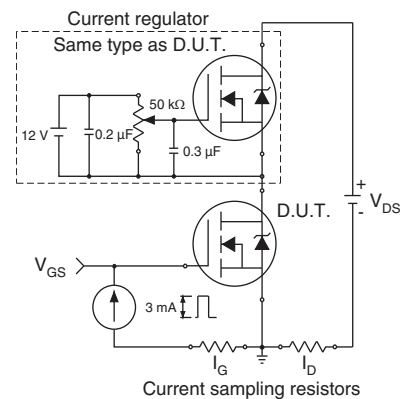
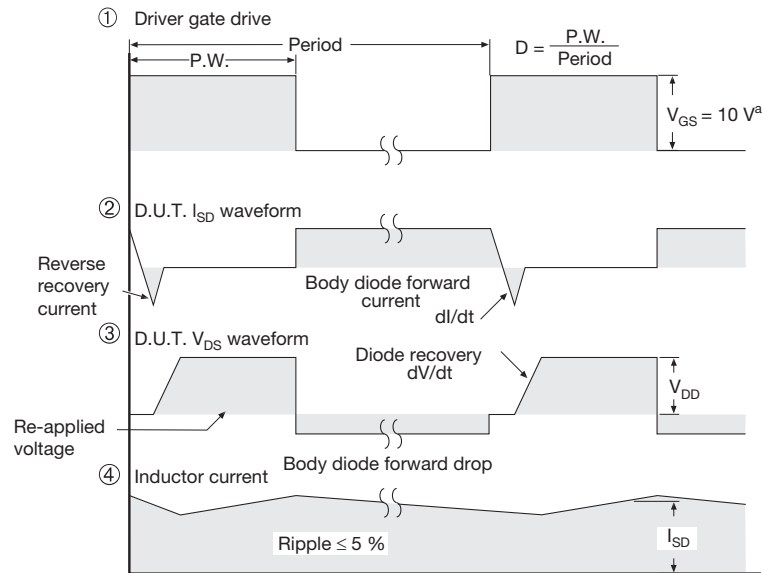
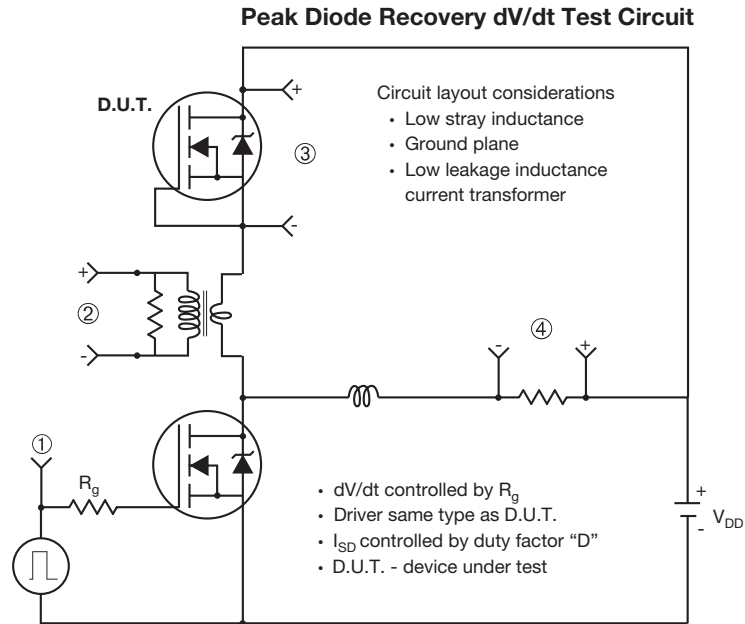


Fig. 13b - Gate Charge Test Circuit

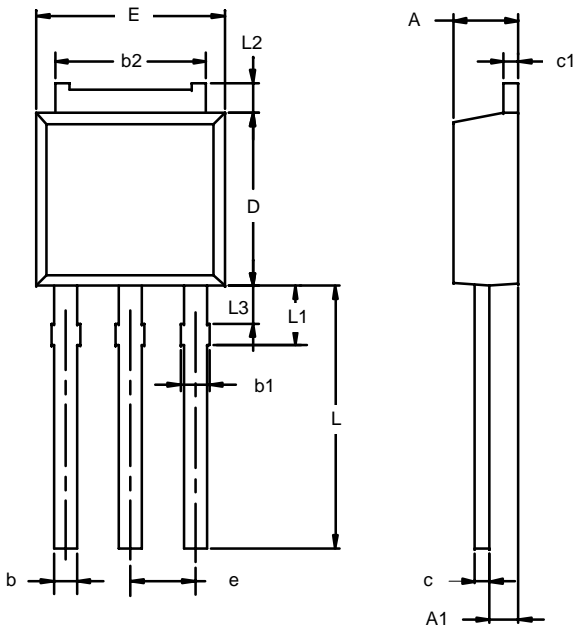


**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

TO-251AA



Note: Dimension L3 is for reference only.

Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	2.21	2.38	0.087	0.094
A1	0.89	1.14	0.035	0.045
b	0.71	0.89	0.028	0.035
b1	0.76	1.14	0.030	0.045
b2	5.23	5.43	0.206	0.214
c	0.46	0.58	0.018	0.023
c1	0.46	0.58	0.018	0.023
D	5.97	6.22	0.235	0.245
E	6.48	6.73	0.255	0.265
e	2.28 BSC		0.090 BSC	
L	3.89	9.53	0.153	0.375
L1	1.91	2.28	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.15	1.52	0.045	0.060



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