

Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	550	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	3.0
Q_g (Max.) (nC)	18	
Q_{gs} (nC)	3.0	
Q_{gd} (nC)	8.9	
Configuration	Single	

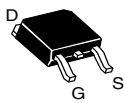
FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Available in Tape and Reel
- Fast Switching
- Ease of Paralleling

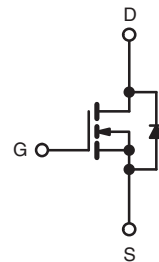
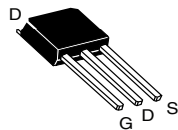


RoHS
COMPLIANT
HALOGEN
FREE
Available

DPAK
(TO-252)



IPAK
(TO-251)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)				
PARAMETER			SYMBOL	LIMIT
Drain-Source Voltage			V_{DS}	550
Gate-Source Voltage			V_{GS}	± 20
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25\text{ }^{\circ}\text{C}$	I_D	2.0
		$T_C = 100\text{ }^{\circ}\text{C}$		1.3
Pulsed Drain Current ^a			I_{DM}	8.0
Linear Derating Factor				0.33
Linear Derating Factor (PCB Mount) ^e				0.020
Single Pulse Avalanche Energy ^b			E_{AS}	74
Repetitive Avalanche Current ^a			I_{AR}	2.0
Repetitive Avalanche Energy ^a			E_{AR}	4.2
Maximum Power Dissipation	$T_C = 25\text{ }^{\circ}\text{C}$		P_D	42
Maximum Power Dissipation (PCB Mount) ^e	$T_A = 25\text{ }^{\circ}\text{C}$			2.5
Peak Diode Recovery dV/dt ^c			dV/dt	3.0
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150
Soldering Recommendations (Peak Temperature) ^d	for 10 s			260

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ }^{\circ}\text{C}$, $L = 37\text{ mH}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 2.0\text{ A}$ (see fig. 12).
- $I_{SD} \leq 2.0\text{ A}$, $dI/dt \leq 40\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^{\circ}\text{C}$.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	-	110	°C/W
Maximum Junction-to-Ambient (PCB Mount) ^a	R_{thJA}	-	-	50	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	-	3.0	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

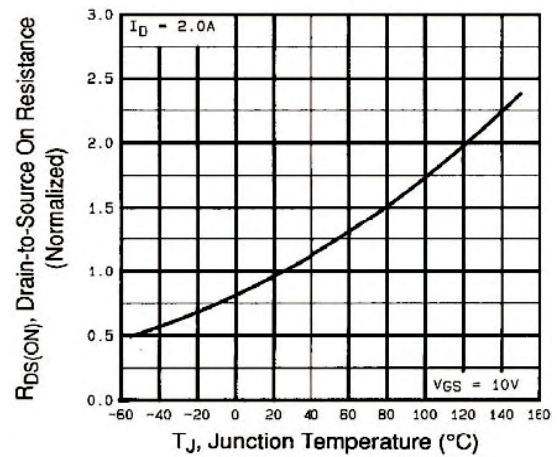
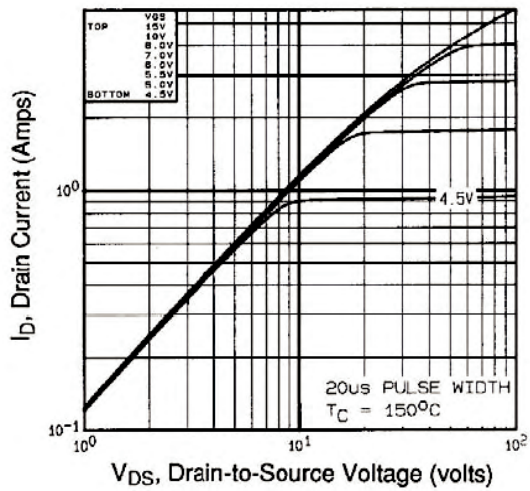
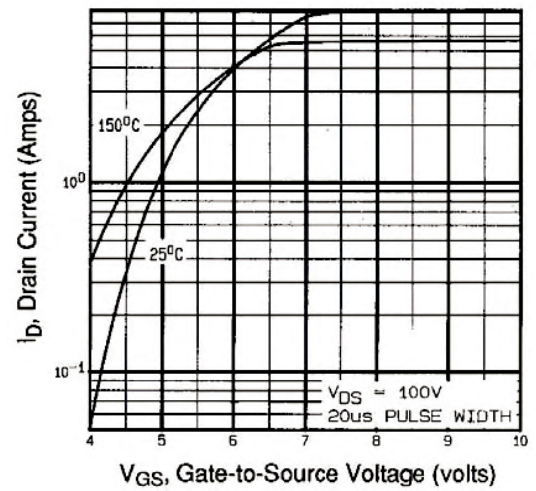
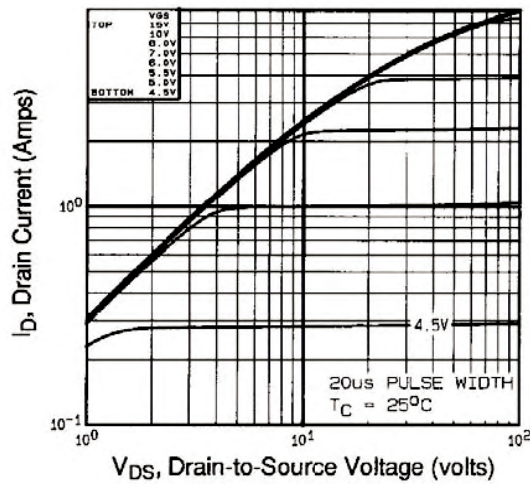
SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		550	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.88	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 550 V, V _{GS} = 0 V		-	-	100	μA
		V _{DS} = 440 V, V _{GS} = 0 V, T _J = 125 °C		-	-	500	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 1.2 A ^b	-	3.0	-	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 1.2 A		1.4	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = - 25 V, f = 1.0 MHz, see fig. 5		-	350	-	pF
Output Capacitance	C _{oss}			-	48	-	
Reverse Transfer Capacitance	C _{rss}			-	8.6	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 2.0 A, V _{DS} = 360 V, see fig. 6 and 13 ^b	-	-	18	nC
Gate-Source Charge	Q _{gs}			-	-	3.0	
Gate-Drain Charge	Q _{gd}			-	-	8.9	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 300 V, I _D = 2.0 A, R _g = 18 Ω, R _D = 135 Ω, see fig. 10 ^b		-	10	-	ns
Rise Time	t _r			-	23	-	
Turn-Off Delay Time	t _{d(off)}			-	30	-	
Fall Time	t _f			-	25	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	2.0	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	8.0	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 2.0 A, V _{GS} = 0 V ^b		-	-	1.6	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 2.0 A, dI/dt = 100 A/μs ^b		-	290	580	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	0.67	1.3	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
 b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



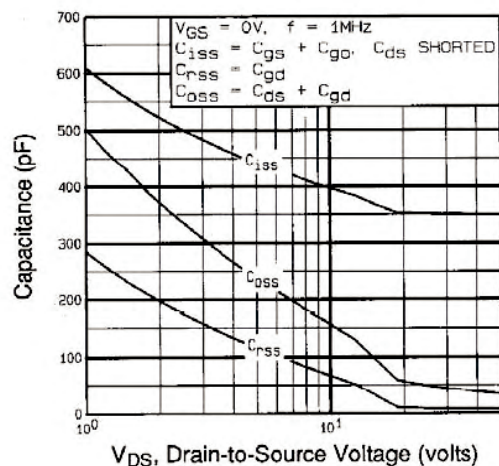


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

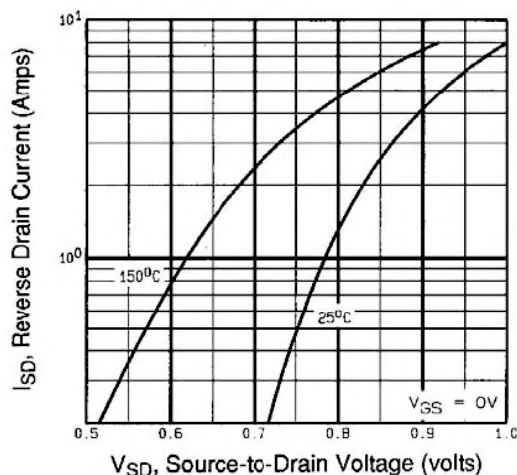


Fig. 7 - Typical Source-Drain Diode Forward Voltage

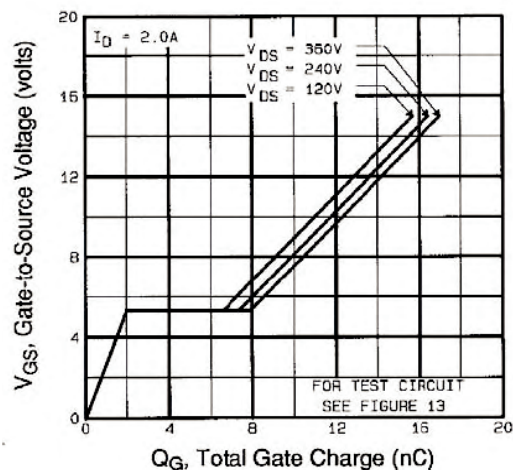


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

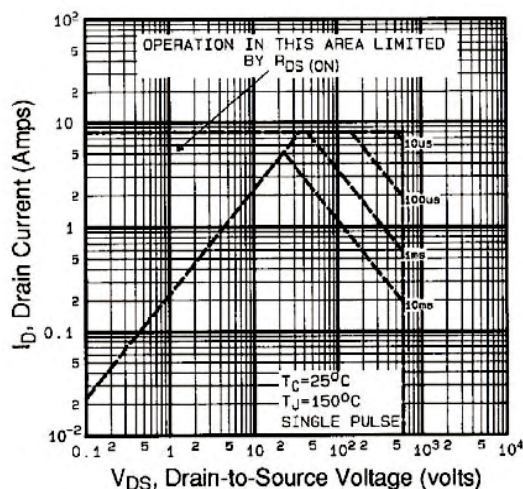


Fig. 8 - Maximum Safe Operating Area

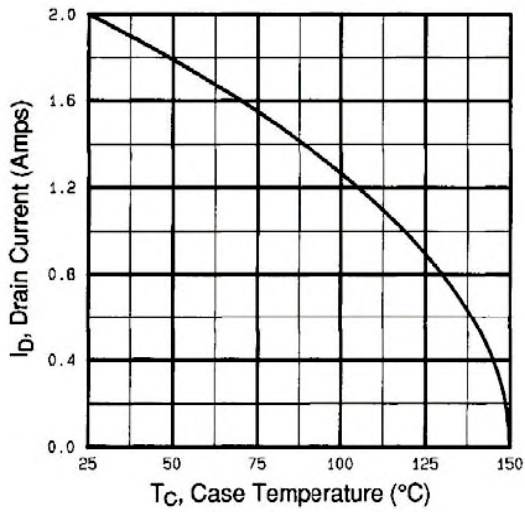


Fig. 9 - Maximum Drain Current vs. Case Temperature

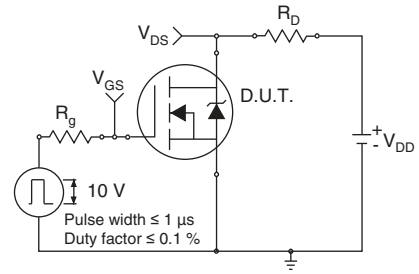


Fig. 10a - Switching Time Test Circuit

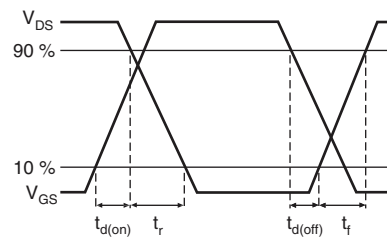


Fig. 10b - Switching Time Waveforms

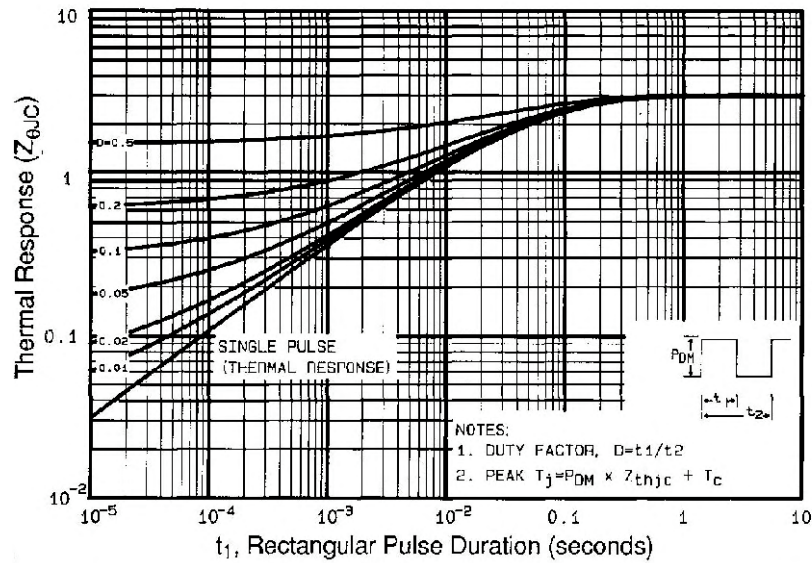


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

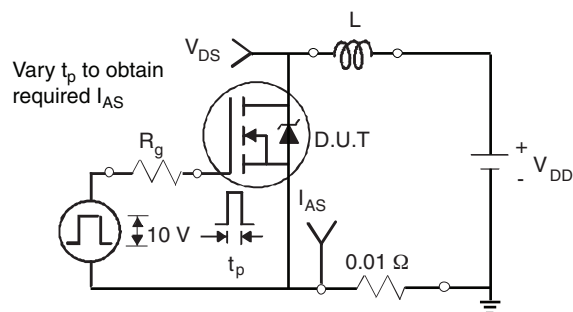


Fig. 12a - Unclamped Inductive Test Circuit

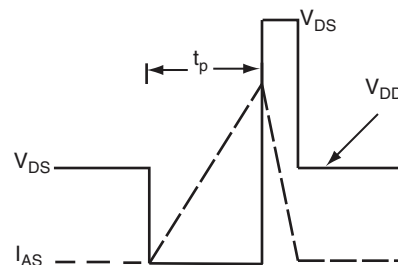


Fig. 12b - Unclamped Inductive Waveforms

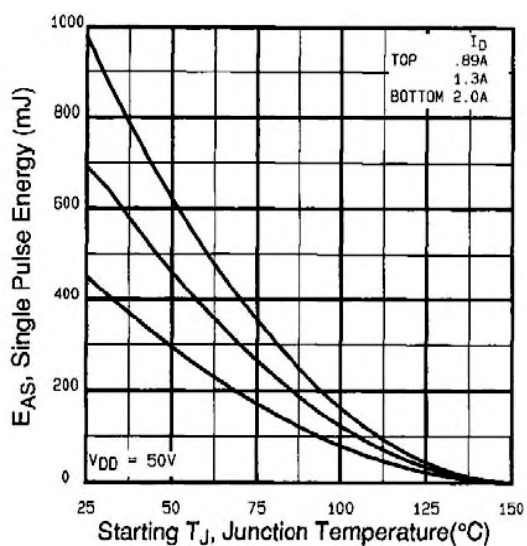


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

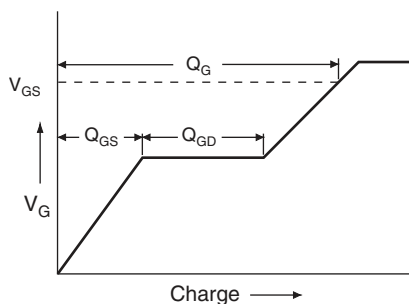


Fig. 13a - Basic Gate Charge Waveform

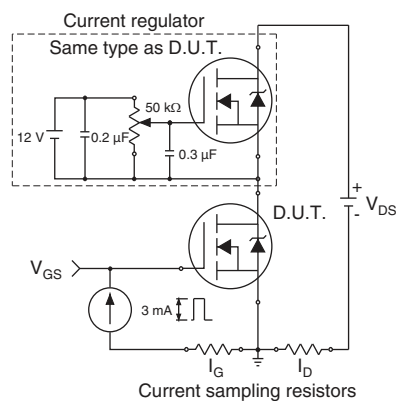
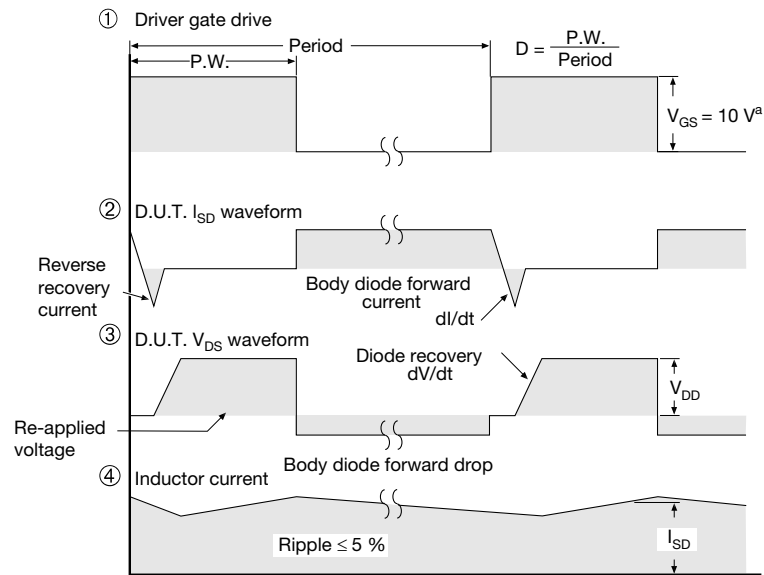
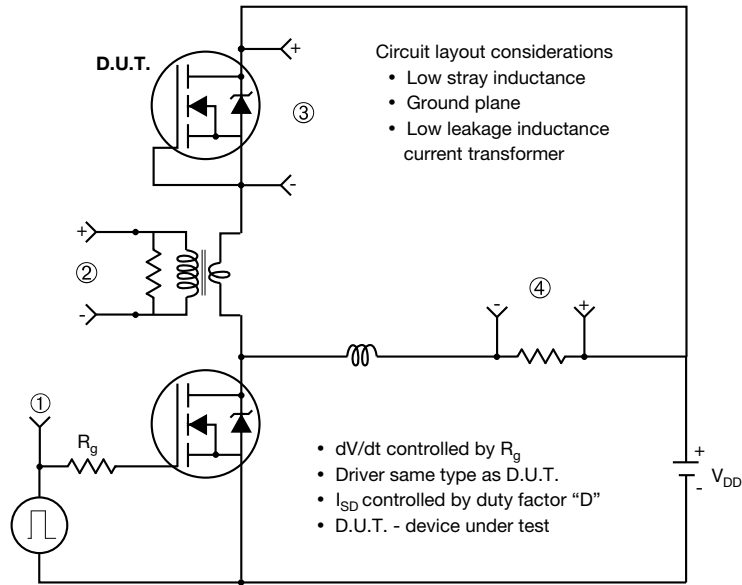


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

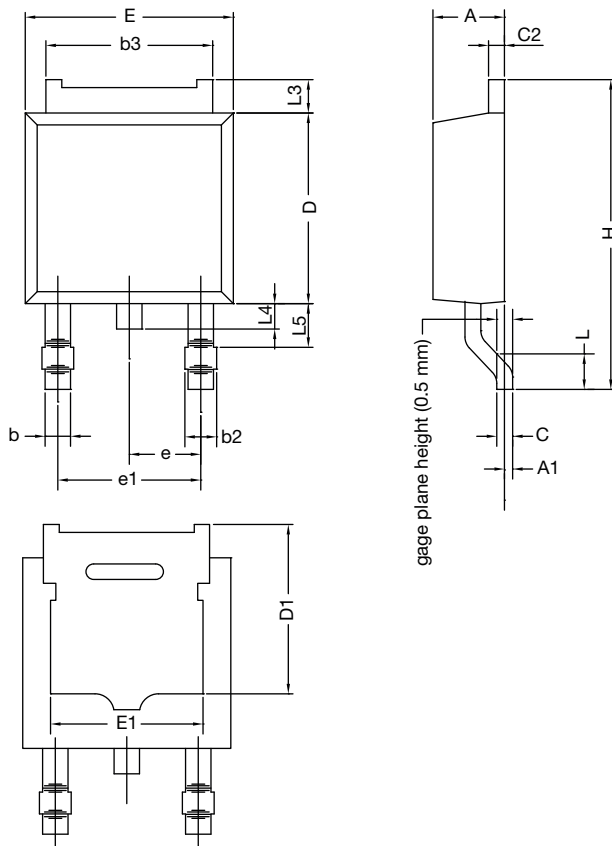


Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

TO-252AA Case Outline

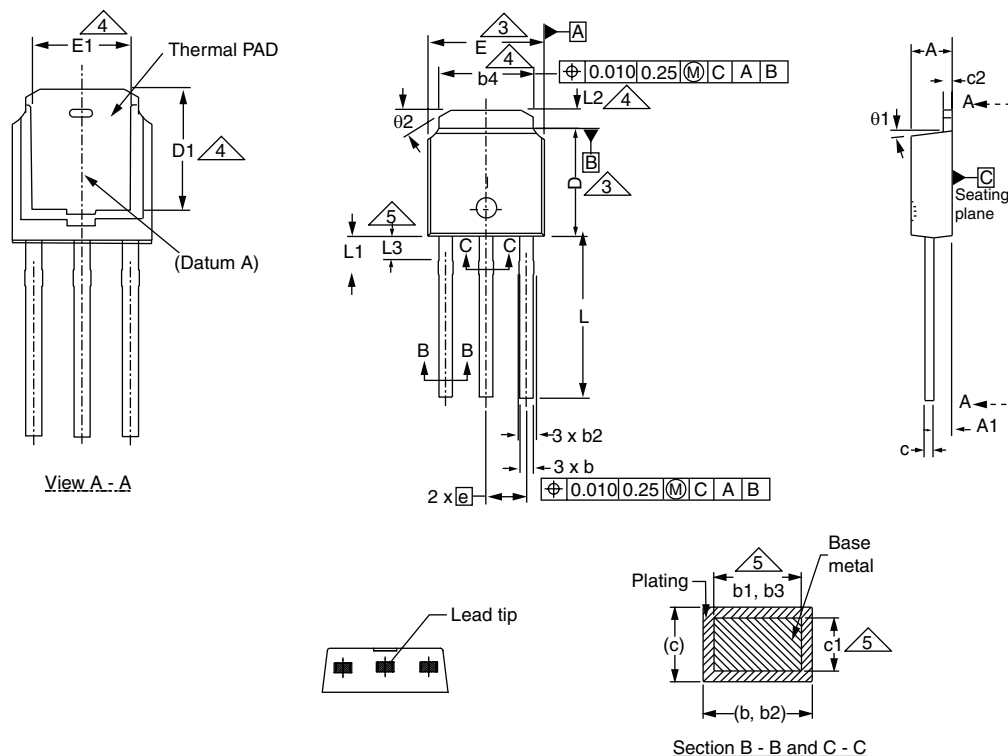


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T16-0236-Rev. P, 16-May-16 DWG: 5347				

Notes

- Dimension L3 is for reference only.

TO-251AA (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1	0.89	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b1	0.65	0.79	0.026	0.031
b2	0.76	1.14	0.030	0.045
b3	0.76	1.04	0.030	0.041
b4	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c1	0.41	0.56	0.016	0.022
c2	0.46	0.86	0.018	0.034
D	5.97	6.22	0.235	0.245

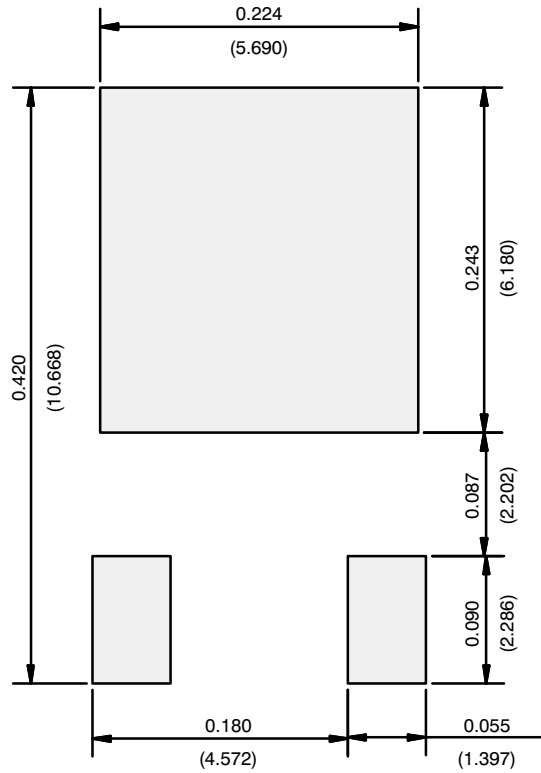
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
e	2.29 BSC		2.29 BSC	
L	8.89	9.65	0.350	0.380
L1	1.91	2.29	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.14	1.52	0.045	0.060
θ1	0°	15°	0°	15°
θ2	25°	35°	25°	35°

ECN: S-82111-Rev. A, 15-Sep-08
DWG: 5968

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension are shown in inches and millimeters.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.13 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions b4, L2, E1 and D1.
5. Lead dimension uncontrolled in L3.
6. Dimension b1, b3 and c1 apply to base metal only.
7. Outline conforms to JEDEC outline TO-251AA.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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