

RoHS COMPLIANT HALOGEN

FREE

# Dual P-Channel 100 V (D-S) MOSFET

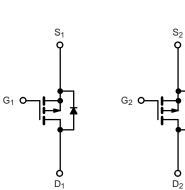
PRODUCT SUMMARY				
V <sub>DS</sub> (V)	-100			
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS}$ = -10 V	0.110			
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS}$ = -4.5 V	0.155			
Q <sub>g</sub> typ. (nC)	5.65			
I <sub>D</sub> (A)	-4.5			
Configuration	Single			

#### **FEATURES**

- Trench power MOSFET
- + 100 %  $\rm R_g$  and UIS tested

#### **APPLICATIONS**

- Active clamp in intermediate DC/DC power supplies
- LED Lighting
- · Load switch



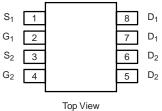
P-Channel MOSFET

P-Channel MOSFET

PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V <sub>DS</sub>	-100 ± 20		
Gate-source voltage		V <sub>GS</sub>			
Continuous drain current (T <sub>J</sub> = 150 °C)	T <sub>C</sub> = 25 °C		-4.5		
	T <sub>C</sub> = 70 °C		-3.6		
	T <sub>A</sub> = 25 °C	I <sub>D</sub>	-2.8 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C		-2.1 <sup>b, c</sup>	•	
Pulsed drain current (t = 100 µs)		I <sub>DM</sub>	-20	A	
Continuous source-drain diode current	T <sub>C</sub> = 25 °C		-4.5 <sup>a</sup>		
	T <sub>A</sub> = 25 °C	I <sub>S</sub>	-2.8 <sup>b, c</sup>		
Single pulse avalanche current		I <sub>AS</sub>	-15		
Single pulse avalanche energy	L = 0.1 mH	E <sub>AS</sub>	11.25	mJ	
Maximum power dissipation	T <sub>C</sub> = 25 °C		27.8		
	T <sub>C</sub> = 70 °C		17.8	w	
	T <sub>A</sub> = 25 °C	P <sub>D</sub>	3.5 <sup>b, c</sup>	vv	
	T <sub>A</sub> = 70 °C		2.2 <sup>b, c</sup>		
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C	
Soldering recommendations (peak temperature) d, e			260	°C	

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient b, f	t $\leq$ 10 s R <sub>thJA</sub> 29		36	°C/W		
Maximum junction-to-case (drain)	Steady state	R <sub>thJC</sub>	3.6	4.6	C/W	





SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)   PARAMETER SYMBOL TEST CONDITIONS MIN. TYP. MAX. UI								
PARAMETER Static	STMBOL	TEST CONDITIONS	IVIIIN.	TYP.	WAX.	UNIT		
	V		-100	-	<u> </u>	V		
Drain-source breakdown voltage	V <sub>DS</sub>	$V_{GS} = 0 V, I_D = -250 \mu A$	-100	-63	-	v		
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = -250 μA			-	mV/°C		
V <sub>GS(th)</sub> temperature coefficient	$\Delta V_{GS(th)}/T_J$		-	4.2	-			
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = -250 \mu A$	-1.1		-2.6	V		
Gate-source leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$	-	-	± 100	nA		
Zero gate voltage drain current	I <sub>DSS</sub>	$V_{DS} = -100 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	-	-1	μΑ		
		$V_{DS} = -100 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 70 \text{ °C}$	-	-	-10			
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge$ -10 V, $V_{GS}$ = -10 V	-15	-	-	A		
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -3.8 A	-	0.110		Ω		
	BO(OII)	$V_{GS} = -4.5 \text{ V}, \text{ I}_{D} = -3.2 \text{ A}$	-	0.155				
Forward transconductance <sup>a</sup>	9 <sub>fs</sub>	$V_{DS} = -10 \text{ V}, \text{ I}_{D} = -3.8 \text{ A}$	-	8	-	S		
Dynamic <sup>b</sup>	P			1		I		
Input capacitance	C <sub>iss</sub>	$V_{DS}$ = -50 V, $V_{GS}$ = 0 V, f = 1 MHz	-	515	-	pF		
Output capacitance	C <sub>oss</sub>		-	162	-			
Reverse transfer capacitance	C <sub>rss</sub>		-	10	-			
Total gate charge	Qg	$V_{\text{DS}}$ = -50 V, $V_{\text{GS}}$ = -10 V, $I_{\text{D}}$ = -3.8 A	-	10.9	16.5	- nC		
Total gate charge	Чg		-	5.65	8.5			
Gate-source charge	Q <sub>gs</sub>	$V_{DS}$ = -50 V, $V_{GS}$ = -4.5 V, $I_D$ = -3.8 A	-	1.7	-			
Gate-drain charge	Q <sub>gd</sub>		-	2.5	-			
Gate resistance	Rg	f = 1 MHz	1.96	9.8	19.6	Ω		
Turn-on delay time	t <sub>d(on)</sub>		-	10	20	-		
Rise time	t <sub>r</sub>	$\begin{split} V_{DD} = -50 \ V, \ R_L &= 16.1 \ \Omega, \ I_D \cong -3.1 \ A, \\ V_{GEN} &= -10 \ V, \ R_g &= 1 \ \Omega \end{split}$	-	22	40			
Turn-off delay time	t <sub>d(off)</sub>		-	20	40			
Fall time	t <sub>f</sub>		-	20	40			
Turn-on delay time	t <sub>d(on)</sub>		-	35	55	ns		
Rise time	tr	$V_{DD}$ = -50 V, R <sub>L</sub> = 16.1 $\Omega$ , I <sub>D</sub> $\cong$ -3.1 A, V <sub>GEN</sub> = -4.5 V, R <sub>g</sub> = 1 $\Omega$	-	40	60	-		
Turn-off delay time	t <sub>d(off)</sub>		-	22	40			
Fall time	t <sub>f</sub>		-	1622	40			
Drain-Source Body Diode Characteristic								
Continuous source-drain diode current	Is	T <sub>C</sub> = 25 °C	-	-	-16			
Pulse diode forward current	I <sub>SM</sub>			-	-15	A		
Body diode voltage	V <sub>SD</sub>	I <sub>S</sub> = -3.1 A, V <sub>GS</sub> = 0 V	-	-0.8	-1.2	V		
Body diode reverse recovery time	t <sub>rr</sub>		-	43	65	ns		
Body diode reverse recovery charge	Q <sub>rr</sub>		-	80	120	nC		
Reverse recovery fall time	t <sub>a</sub>	I <sub>F</sub> = -3.1 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C	-	36	-	- ns		
Reverse recovery rise time	t <sub>b</sub>	4		7	_			

#### Notes

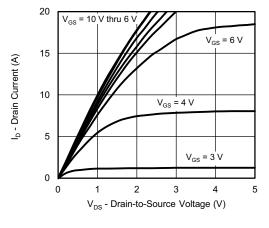
a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %

b. Guaranteed by design, not subject to production testing

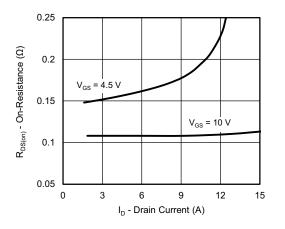
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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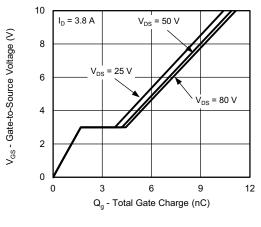




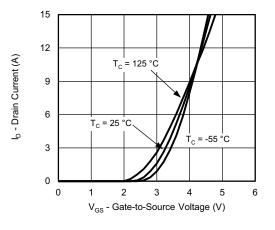
**Output Characteristics** 



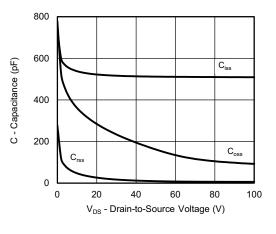
**On-Resistance vs. Drain Current and Gate Voltage** 



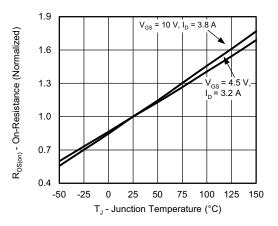
Gate Charge



**Transfer Characteristics** 

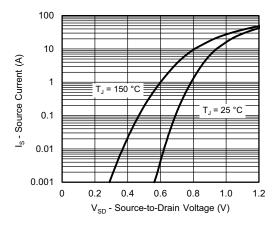


Capacitance

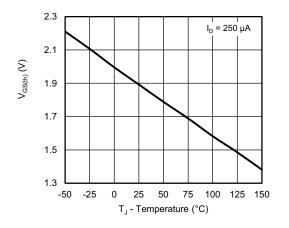


**On-Resistance vs. Junction Temperature** 

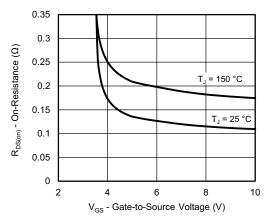




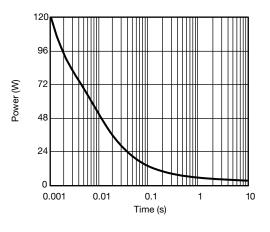
Source-Drain Diode Forward Voltage



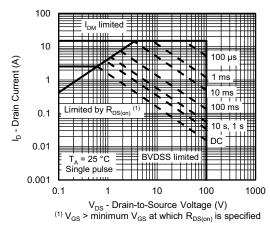
**Threshold Voltage** 



**On-Resistance vs. Gate-to-Source Voltage** 

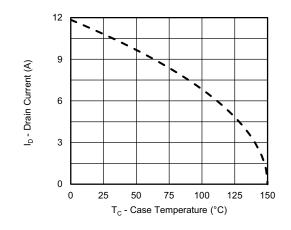


Single Pulse Power, Junction-to-Ambient

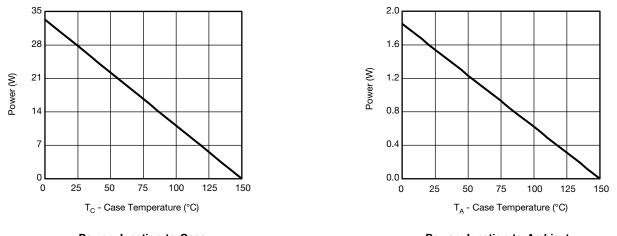


Safe Operating Area, Junction-to-Ambient





Current Derating <sup>a</sup>



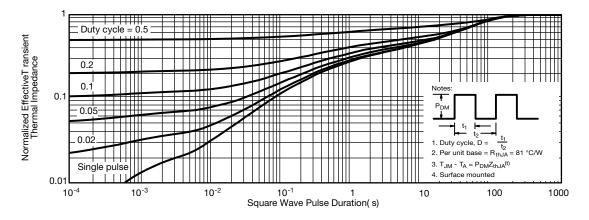
Power, Junction-to-Case

Power, Junction-to-Ambient

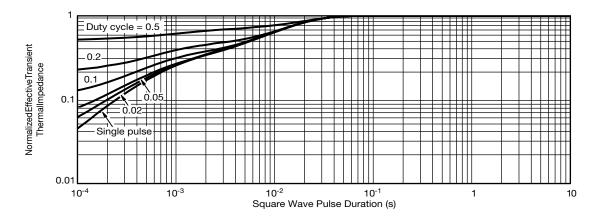
#### Note

a. The power dissipation P<sub>D</sub> is based on T<sub>J</sub> max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case



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