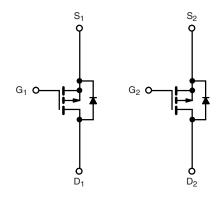


F7754-VB Datasheet

Dual P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A) ^d	Q _g (Typ.)	
	0.013 at $V_{GS} = -4.5 \text{ V}$	-7.5		
- 20	0.018 at V _{GS} = - 2.5 V	-6.5	20 nC	
	0.032 at V _{GS} = - 1.8 V	-5.0		



P-Channel MOSFET

P-Channel MOSFET

FEATURES

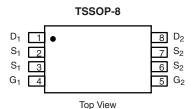
- Halogen-free According to IEC 61249-2-21 Definition
- Trench Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC



ROHS COMPLIANT HALOGEN FREE

APPLICATIONS

- · Adaptor Switch
- High Current Load Switch
- Notebook



ABSOLUTE MAXIMUM RATINGS	TA = 25 O, unless our			1
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	- 20	V	
Gate-Source Voltage		V_{GS}	± 12	v
	T _C = 25 °C		- 7.5	
Continuous Drain Current /T 150 °C)	T _C = 70 °C		- 6.0	
Continuous Drain Current (T _J = 150 °C)	T _A = 25 °C	I _D	- 5.4 ^{a, b}	
	T _A = 70 °C		- 4.5 ^{a, b}	Α .
Pulsed Drain Current		I _{DM}	- 30	A
Ocation of Ocata	T _C = 25 °C		- 4.1	
Continuous Source-Drain Diode Current	T _A = 25 °C	l _S	- 2.1 ^{a, b}	
Avalanche Current	L = 0.1 mH	I _{AS}	- 15	
Single-Pulse Avalanche Energy	L = 0.1 IIII	E _{AS}	11.25	mJ
	T _C = 25 °C		5	
Maximum Power Dissipation	T _C = 70 °C		3.2	w
	T _A = 25 °C	P _D	2.5 ^{a, b}	VV
	T _A = 70 °C		1.6 ^{a, b}	
Operating Junction and Storage Temperature Range		T _J , T _{stq}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{a, c}	t ≤ 10 s	R _{thJA}	38	50	°C/W	
Maximum Junction-to-Foot	Steady State	R _{th,IF}	20	25	- C/VV	

Notes:

- a. Surface mounted on 1" x 1" FR4 board.
- b. t = 10 s.
- c. Maximum under steady state conditions is 85 $^{\circ}\text{C/W}.$
- d. Based on $T_C = 25$ °C.



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	- 20			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = - 250 μA		- 14.5		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			2.8			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 0.4		- 1.0	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$			± 100	nA	
Zara Cata Valtaga Drain Corrent	I _{DSS}	V _{DS} = - 20 V, V _{GS} = 0 V			- 1	μΑ	
Zero Gate Voltage Drain Current		V _{DS} = - 20 V, V _{GS} = 0 V, T _J = 70 °C			- 10		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge -10 \text{ V}, V_{GS} = -5 \text{ V}$	- 20			Α	
	, ,	V _{GS} = - 4.5 V, I _D = - 7 A		0.013		1	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 2.5 V, I _D = - 6 A		0.018		Ω	
	- (-)	V _{GS} = - 1.8 V, I _D = - 3 A		0.032			
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 10 V, I _D = - 9 A		40		S	
Dynamic ^b		, = - ,					
Input Capacitance	C _{iss}			2380			
Output Capacitance	C _{oss}	V _{DS} = - 10 V, V _{GS} = 0 V, f = 1 MHz		340		pF	
Reverse Transfer Capacitance	C _{rss}	1		280			
	Q _g Q _{gs} Q _{ad}	V _{DS} = - 10 V, V _{GS} = - 8 V, I _D = - 5 A		45	70	nC	
Total Gate Charge		V _{DS} = - 10 V, V _{GS} = - 4.5 V, I _D = - 5 A		20	35		
Gate-Source Charge				3.1			
Gate-Drain Charge				8.4			
Gate Resistance	R _q	f = 1 MHz	1.0	4.8	9.6	Ω	
Turn-On Delay Time	t _{d(on)}			7	14		
Rise Time	t _r	V_{DD} = - 10 V, R_L = 2 Ω $I_D \cong$ - 5 A, V_{GEN} = - 8 V, R_g = 1 Ω		9	18		
Turn-Off DelayTime	t _{d(off)}			108	200		
Fall Time	t _f			41	80		
Turn-On Delay Time t _d				14	28	ns	
Rise Time				16	32		
Turn-Off DelayTime	t _{d(off)}	$V_{DD} = -10 \text{ V}, R_L = 2 \Omega$ $I_D \cong -5 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_g = 1 \Omega$		101	200		
Fall Time	t _f			40	80		
Drain-Source Body Diode Characteris				<u> </u>			
Continous Source-Drain Diode Current	I _S	T _C = 25 °C			- 4.1		
Pulse Diode Forward Current	I _{SM}	Ŭ			- 40	A	
Body Diode Voltage	V _{SD}	I _S = - 3 A, V _{GS} = 0 V		- 0.66	- 1.2	V	
Body Diode Reverse Recovery Time	t _{rr}	5 · 40		81	150	ns	
Body Diode Reverse Recovery Charge Q _{rr}		1		150	300	nC	
Reverse Recovery Fall Time	t _a	$I_F = -2.3 \text{ A, dI/dt} = 100 \text{ A/}\mu\text{s, T}_J = 25 ^{\circ}\text{C}$		43		ns	
Reverse Recovery Rise Time	t _b	-		38			

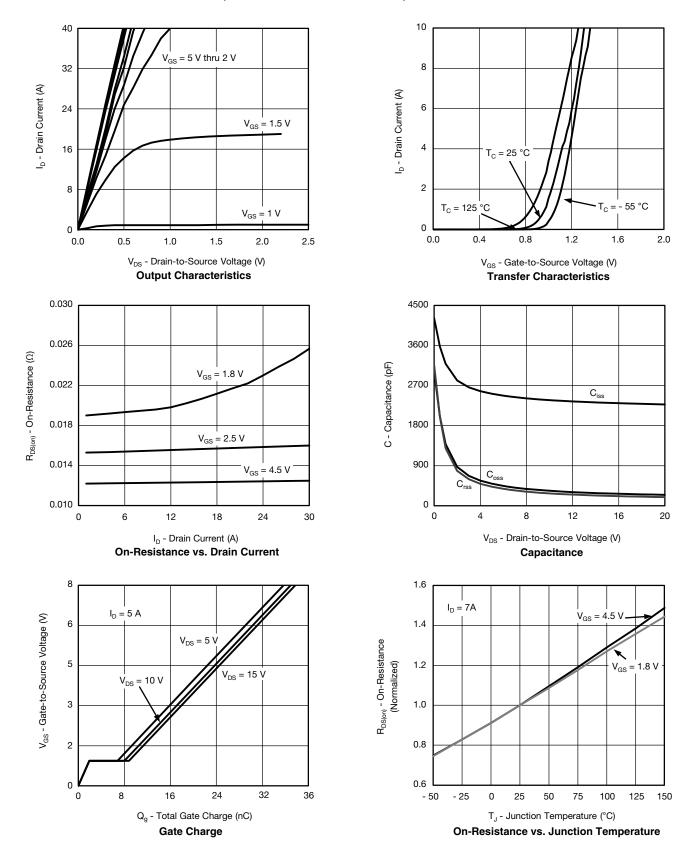
Notes:

2

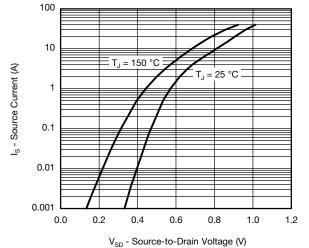
- a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

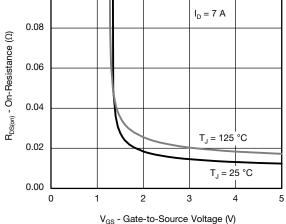






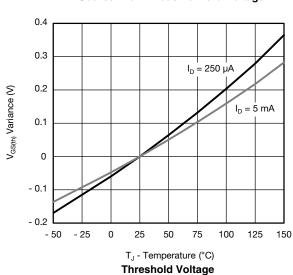


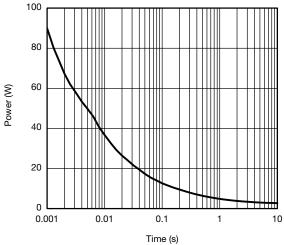
Source-Drain Diode Forward Voltage



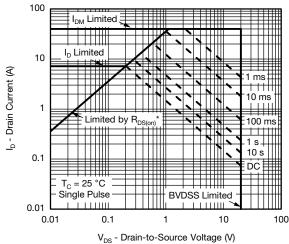
0.10

On-Resistance vs. Gate-to-Source Voltage





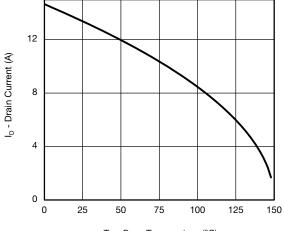
Single Pulse Power, Junction-to-Ambient



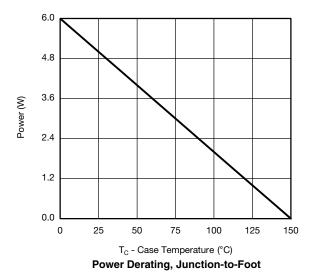
* V_{GS} > minimum V_{GS} at which R_{DS(on)} is specified

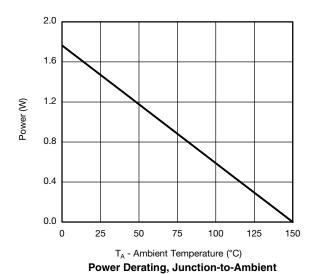
Safe Operating Area





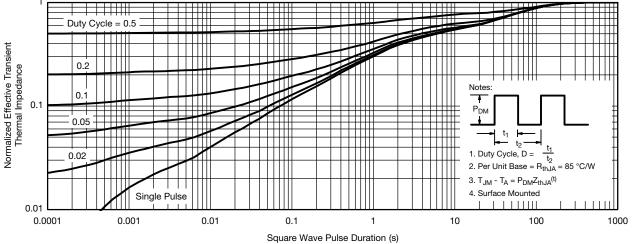
T_C - Case Temperature (°C) **Current Derating***



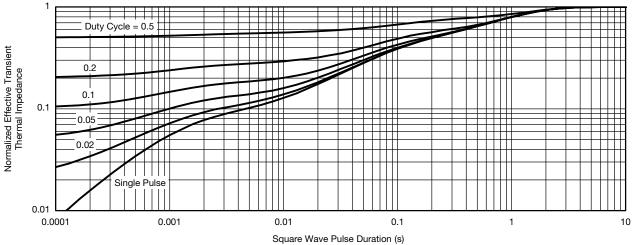


^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot



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