

IPTC026N12NM6ATMA1-VB Datasheet

N-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω) MAX.	I_D (A)	Q_g (TYP.)
100	0.0012 at $V_{GS} = 10$ V	415	130 nC

FEATURES

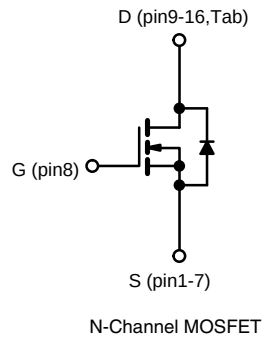
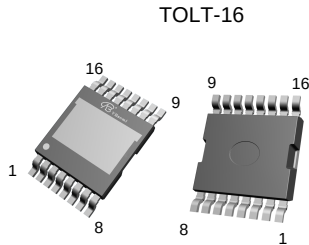
- SGT technology Power MOSFET
- Maximum 175°C junction temperature
- 100 % R_g and UIS tested



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Power supplies:
 - Uninterruptible power supplies
 - AC/DC switch-mode power supplies
 - Lighting
- Synchronous rectification
- DC/DC converter
- Motor drive switch
- DC/AC inverter
- Solar micro inverter
- Class D audio amplifier



ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	$T_C = 25^\circ\text{C}$	I_D	415	A
	$T_C = 100^\circ\text{C}$		296	
Pulsed Drain Current ($t = 100\ \mu\text{s}$)		I_{DM}	1500	
Avalanche Current	$L = 0.5\ \text{mH}$	I_{AS}	100	
Single Avalanche Energy ^a		E_{AS}	2500	mJ
Maximum Power Dissipation ^a	$T_C = 25^\circ\text{C}$	P_D	455 ^b	W
	$T_C = 100^\circ\text{C}$		227 ^b	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient (PCB Mount) ^c	R_{thJA}	62	$^\circ\text{C/W}$
Junction-to-Case (Drain)	R_{thJC}	0.33	

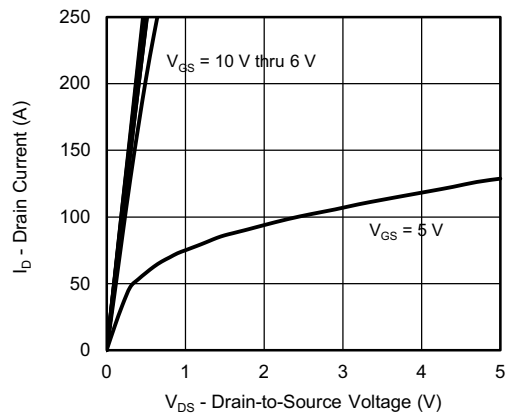
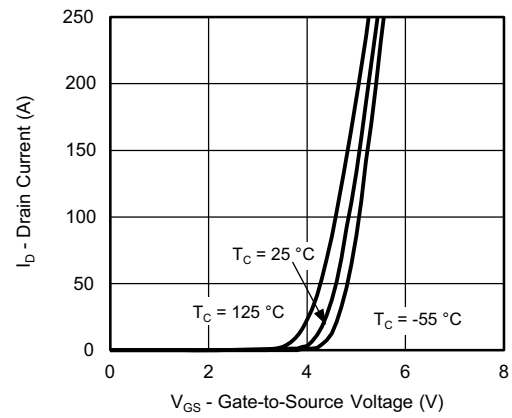
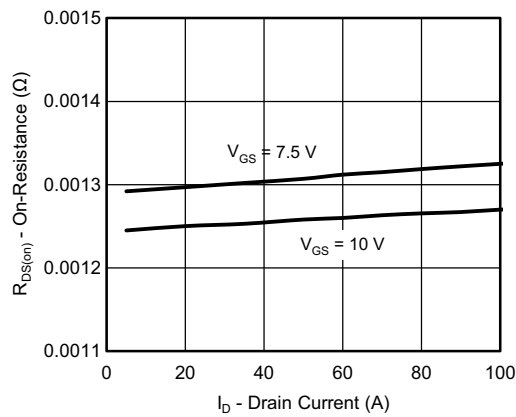
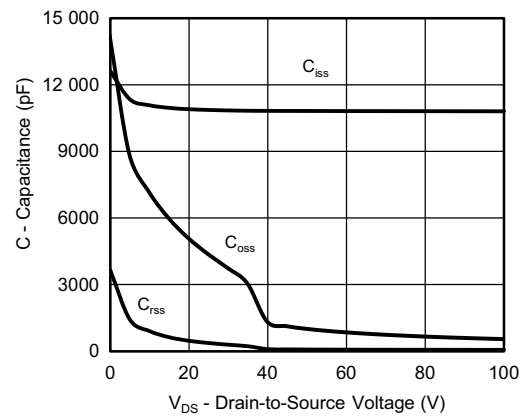
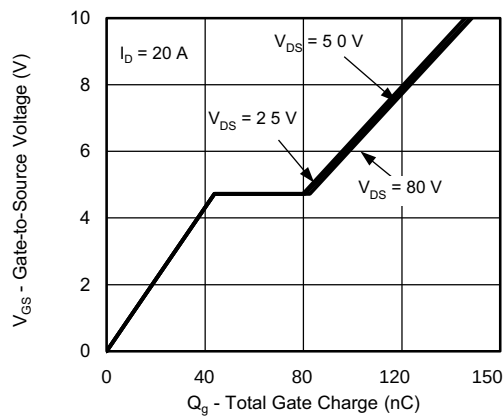
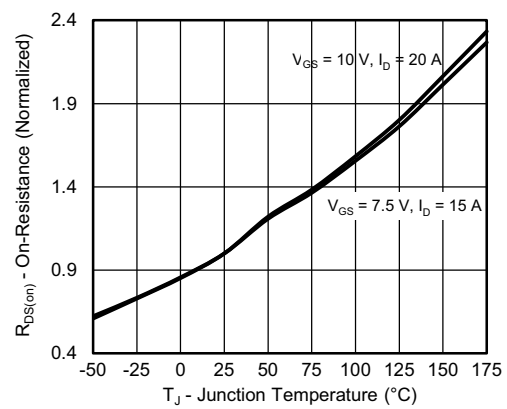
Notes

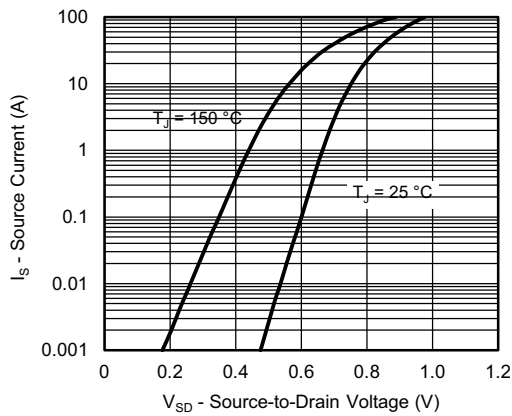
- Duty cycle $\leq 1\%$.
- See SOA curve for voltage derating.
- When mounted on 1" square PCB (FR4 material).

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	100	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2	3	4	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	± 250	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 125 °C	-	-	100	
		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 150°C	-	-	5	mA
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 10 V, V _{GS} = 10 V	150	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 60 A	-	0.0012	-	Ω
		V _{GS} = 7.5 V, I _D = 50 A	-	0.0015	-	
Forward Transconductance ^a	g _{fs}	V _{DS} = 25 V, I _D = 100 A	-	260	-	S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 50 V, f = 1 MHz	-	11500	-	pF
Output Capacitance	C _{oss}		-	3246	-	
Reverse Transfer Capacitance	C _{rss}		-	18	-	
Total Gate Charge ^c	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 20 A	-	130	-	nC
Gate-Source Charge ^c	Q _{gs}		-	50	-	
Gate-Drain Charge ^c	Q _{gd}		-	30	55	
Gate Resistance	R _g	f = 1 MHz	-	0.8	1.2	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 50 V, R _L = 5 Ω I _D ≅ 50 A, V _{GEN} = 10 V, R _g = 1 Ω	-	33	-	ns
Rise Time ^c	t _r		-	30	-	
Turn-Off Delay Time ^c	t _{d(off)}		-	50	-	
Fall Time ^c	t _f		-	55	-	
Drain-Source Body Diode Ratings and Characteristics ^b (T _C = 25 °C)						
Pulsed Current (t = 100 μs)	I _{SM}		-	-	480	A
Forward Voltage ^a	V _{SD}	I _F = 500 A, V _{GS} = 0 V	-	0.75	1.2	V
Reverse Recovery Time	t _{rr}	I _F = 50 A, di/dt = 100 A/μs	-	140	280	ns
Peak Reverse Recovery Charge	I _{RM(REC)}		-	11	20	A
Reverse Recovery Charge	Q _{rr}		-	0.3	0.8	μC

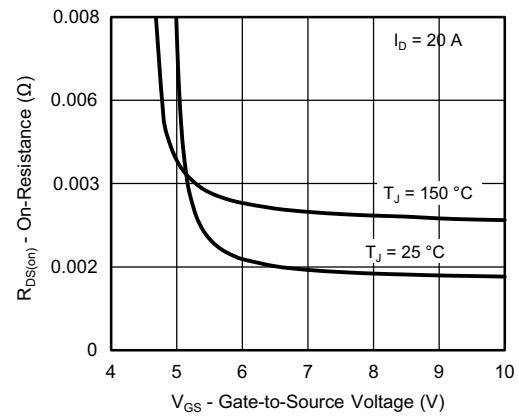
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.
 c. Independent of operating temperature.

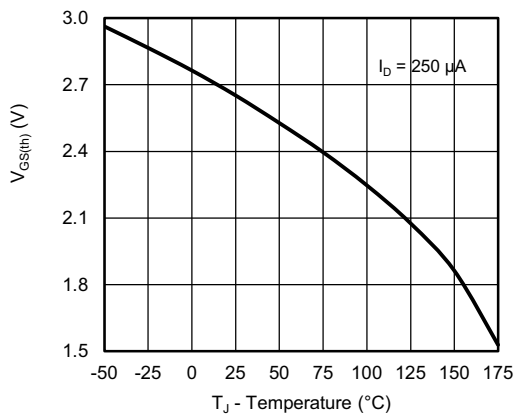
TYPICAL CHARACTERISTICS ($T_C = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature



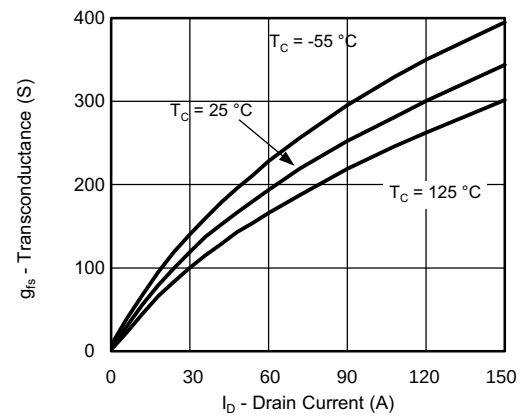
Source-Drain Diode Forward Voltage



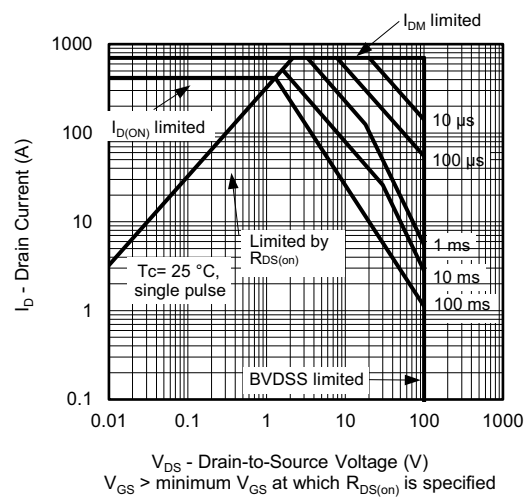
On-Resistance vs. Gate-to-Source Voltage



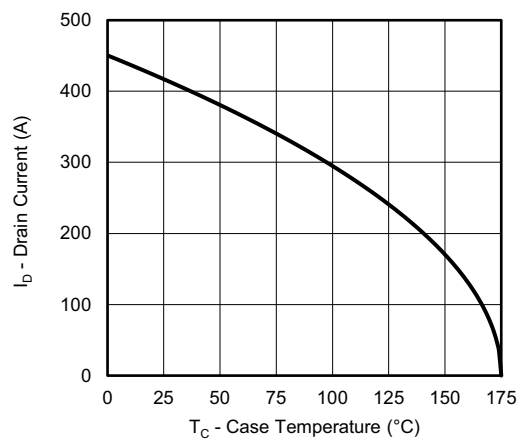
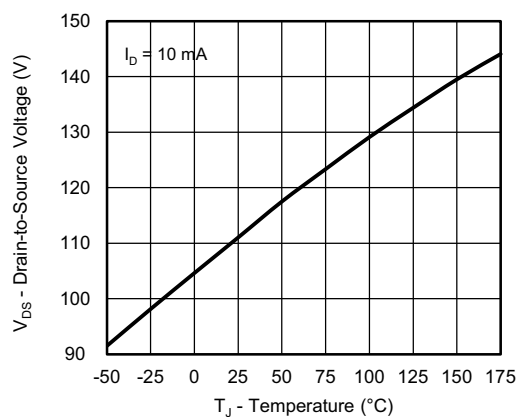
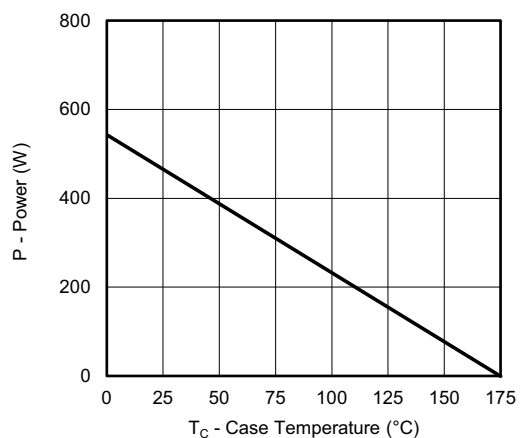
Threshold Voltage



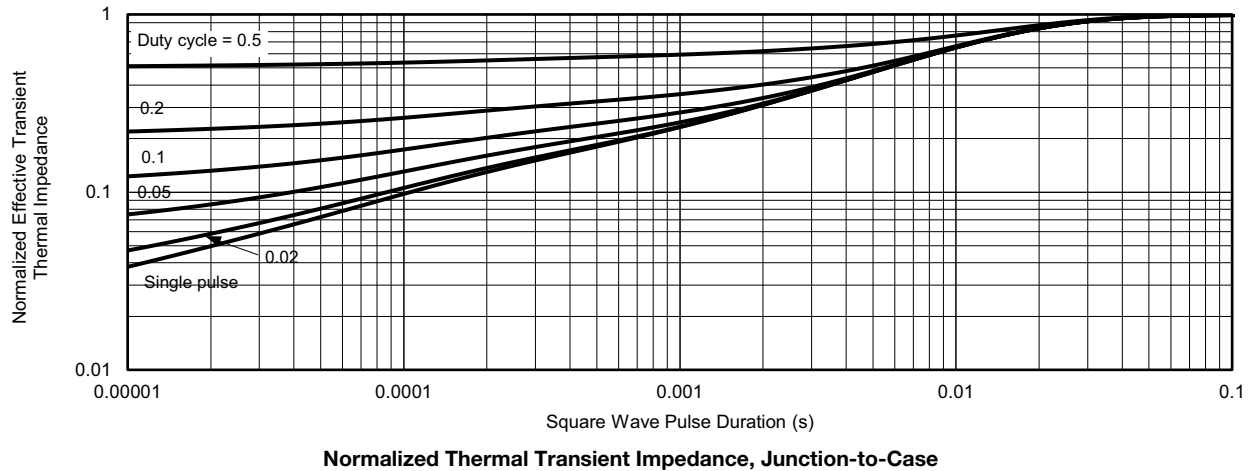
Transconductance



Safe Operating Area, Junction-to-Ambient

**Current Derating ^a****Drain Source Breakdown vs. Junction Temperature****Power, Junction-to-Case****Note**

- a. The power dissipation P_D is based on T_J max. = 25 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

THERMAL RATINGS ($T_C = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction to Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction to Case ($25\text{ }^{\circ}\text{C}$)
 are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Technical drawing of a 16-pin D-subminiature connector, showing three views: front, side, and detail.

Front View (Left): Shows the connector housing with dimensions E (total width), $E1$ (pin width), $E3$ (internal width), and $E4$ (internal width). The overall height is $D1$. The pin pitch is e . The pin-1 mark is indicated. The housing thickness is L . The pin array is $b \times 4$ and $b1 \times 12$. The housing depth is $D2$ and $D3$.

Side View (Middle): Shows the connector profile with dimensions A (top flange width), $A1$ (top flange thickness), D (overall height), and C (bottom flange thickness). The pin array is 18° and 2 ± 0.28 .

Detail View (Right): Shows the pin array with dimensions $E2$ (pin width), H (pin height), $H1$ (pin height), and p (pin pitch). The pin array is $b1$.

Detail View (Bottom): Shows the pin array with dimensions $A2$ (pin height), $A3$ (pin width), and angles $\theta1$ and $\theta2$. The pin array is $2:1$.

SYMBOLS	A	A1	A2	A3	b	b1	C	D
MIN	2.25	1.00	0.01	1.50REF	0.68	0.75	0.45	14.80
NOM	2.30	1.04	0.08		0.70	0.85	0.50	15.00
MAX	2.35	1.08	0.16		0.74	0.95	0.55	15.20
SYMBOLS	D1	D2	D3	E	E1	E2	E3	E4
MIN	10.00	2.40	5.77REF	9.70	9.46REF	9.25REF	8.25REF	8.70REF
NOM	10.10	2.60		9.90				
MAX	10.30	2.80		10.10				
SYMBOLS	e	H	H1	L	P	ϕ1	ϕ2	
MIN	1.18	5.00	4.40	2.40	2.80	7 °	7 °	
NOM	1.20	5.20	4.60	2.45	3.00	-	-	
MAX	1.22	5.40	4.80	2.50	3.20	9 °	9 °	

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