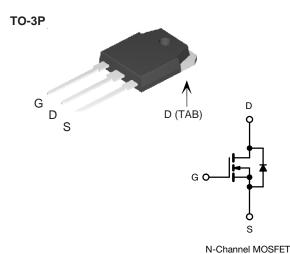


### SSH22N50A-VB Datasheet

## N-Channel 600 V (D-S) Super Junction MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V) at T <sub>J</sub> max.	600			
R <sub>DS(on)</sub> (Ω) at 25 °C	V <sub>GS</sub> = 10 V	0.19		
Q <sub>g</sub> max. (nC)	106			
Q <sub>gs</sub> (nC)	14			
Q <sub>gd</sub> (nC)	33			
Configuration	Single			



#### **FEATURES**

- Reduced t<sub>rr</sub>, Q<sub>rr</sub>, and I<sub>RRM</sub>
- Low figure-of-merit (FOM) Ron x Qg
- Low input capacitance (Ciss)
- Low switching losses due to reduced Q<sub>rr</sub>
- Ultra low gate charge (Q<sub>a</sub>)
- Avalanche energy rated (UIS)

# **HALOGEN FREE**

#### **APPLICATIONS**

- Telecommunications
  - Server and telecom power supplies
- - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- · Consumer and computing
  - ATX power supplies
- Industrial
  - Welding
  - Battery chargers
- Renewable energy
  - Solar (PV inverters)
- Switch mode power supplies (SMPS)

<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>C</sub> = 25 °C, unless otherwise noted)						
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V <sub>DS</sub>	600	V	
Gate-Source Voltage			$V_{GS}$	± 30	v I	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C T <sub>C</sub> = 100 °C	- I <sub>D</sub>	20		
	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 100 °C		13	Α	
Pulsed Drain Current <sup>a</sup>			I <sub>DM</sub>	53		
Linear Derating Factor				1.7	W/°C	
Single Pulse Avalanche Energy b			E <sub>AS</sub>	367	mJ	
Maximum Power Dissipation			$P_{D}$	208	W	
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C	
Drain-Source Voltage Slope	T <sub>J</sub> = 125 °C		dV/dt 37	37	V/ns	
Reverse Diode dV/dt <sup>d</sup>		αν/αι	31	V/IIS		
Soldering Recommendations (Peak Temperature) c	for 10 s			300	°C	

- a. Repetitive rating; pulse width limited by maximum junction temperature. b.  $V_{DD}=50$  V, starting  $T_J=25$  °C, L=28.2 mH,  $R_g=25$   $\Omega$ ,  $I_{AS}=5.1$  A.
- c. 1.6 mm from case.
- d.  $I_{SD} \le I_D$ , dI/dt = 100 A/ $\mu$ s, starting  $T_J = 25$  °C.



THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	R <sub>thJA</sub>	-	62	°C/W	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.5	G/ VV	

PARAMETER	SYMBOL	TES	T CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static		_		l	_	l .	
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		600	-	-	V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.67	-	V/°C
Gate-Source Threshold Voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2	-	4	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
			V <sub>GS</sub> = ± 30 V		-	± 1	μΑ
7 0 1 1/1 5 1 0 1		$V_{DS} = 520 \text{ V}, V_{GS} = 0 \text{ V}$		-	-	1	μΑ
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 520 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	500	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 11 A	-	0.19	-	Ω
Forward Transconductance	9 <sub>fs</sub>	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 11 A		-	7.0	-	S
Dynamic							•
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 100 V, f = 1 MHz			2322	-	pF
Output Capacitance	C <sub>oss</sub>			-	105	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	4	-	
Effective Output Capacitance, Energy Related <sup>a</sup>	C <sub>o(er)</sub>	V <sub>DS</sub> = 0 V to 520 V, V <sub>GS</sub> = 0 V		-	84	-	
Effective Output Capacitance, Time Related <sup>b</sup>	C <sub>o(tr)</sub>			-	293	-	
Total Gate Charge	Qg			-	71	106	
Gate-Source Charge	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V		=.	14	-	nC
Gate-Drain Charge	Q <sub>gd</sub>	1			33	-	
Turn-On Delay Time	t <sub>d(on)</sub>	$V_{DD} = 520 \text{ V}, I_{D} = 11 \text{ A},$ $V_{GS} = 10 \text{ V}, R_{g} = 9.1 \Omega$		-	22	44	ns
Rise Time	t <sub>r</sub>			=.	34	68	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	68	102	
Fall Time	t <sub>f</sub>			-	42	84	
Gate Input Resistance	R <sub>g</sub>	f = 1 MHz, open drain		-	0.78	-	Ω
<b>Drain-Source Body Diode Characteristic</b>	S						
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	21	
Pulsed Diode Forward Current	I <sub>SM</sub>			-	-	53	- A
Diode Forward Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 11 A, V <sub>GS</sub> = 0 V		-	0.9	1.2	V
Reverse Recovery Time	t <sub>rr</sub>	$T_J = 25 \text{ °C}, I_F = I_S = 11 \text{ A},$ $dI/dt = 100 \text{ A/µs}, V_R = 25 \text{ V}$		-	160	-	ns
Reverse Recovery Charge	Q <sub>rr</sub>			-	1.2	-	μC
Reverse Recovery Current	I <sub>RRM</sub>			_	14	_	A

#### Notes

- a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ . b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .



#### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

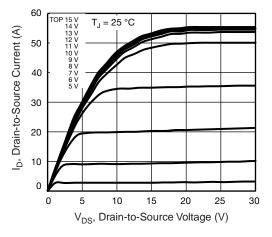


Fig. 1 - Typical Output Characteristics

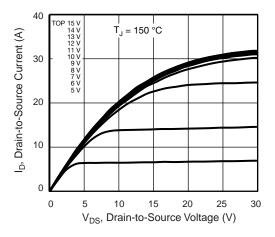


Fig. 2 - Typical Output Characteristics

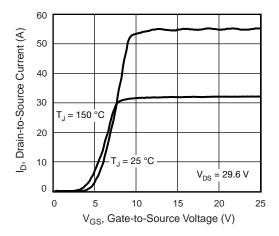


Fig. 3 - Typical Transfer Characteristics

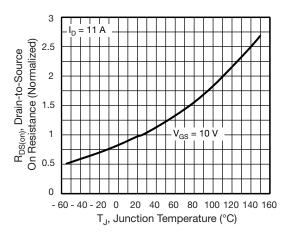


Fig. 4 - Normalized On-Resistance vs. Temperature

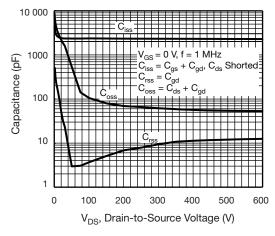


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

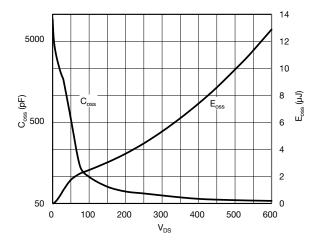


Fig. 6 -  $C_{\text{oss}}$  and  $E_{\text{oss}}$  vs.  $V_{\text{DS}}$ 



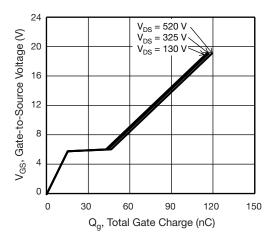


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

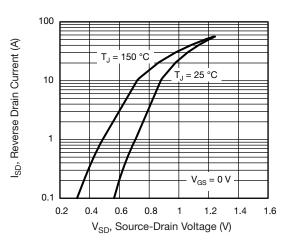


Fig. 8 - Typical Source-Drain Diode Forward Voltage

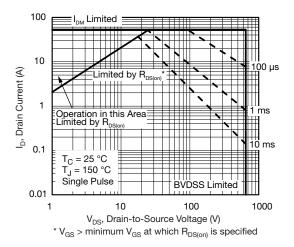


Fig. 9 - Maximum Safe Operating Area

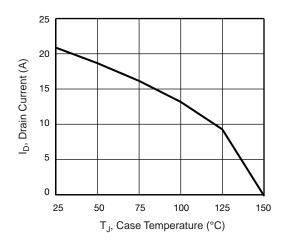


Fig. 10 - Maximum Drain Current vs. Case Temperature

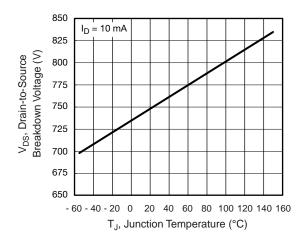


Fig. 11 - Temperature vs. Drain-to-Source Voltage



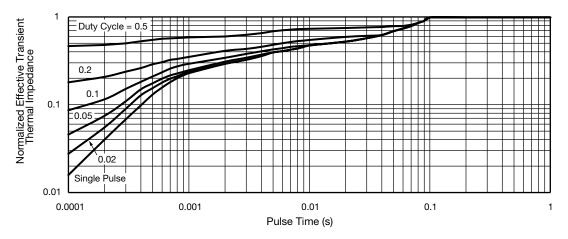


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

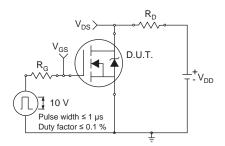


Fig. 13 - Switching Time Test Circuit

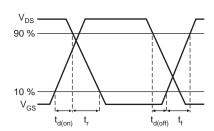


Fig. 14 - Switching Time Waveforms

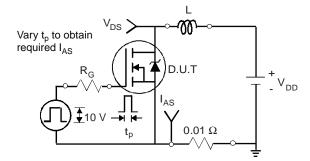


Fig. 15 - Unclamped Inductive Test Circuit

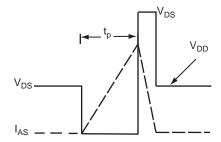


Fig. 16 - Unclamped Inductive Waveforms

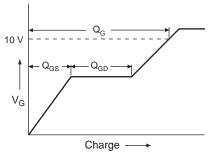


Fig. 17 - Basic Gate Charge Waveform

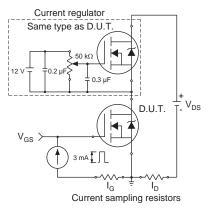
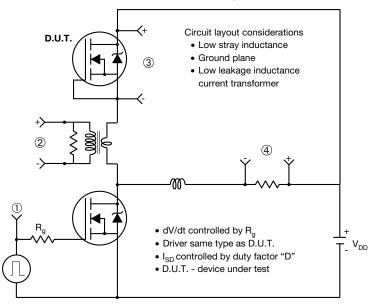


Fig. 18 - Gate Charge Test Circuit



#### Peak Diode Recovery dV/dt Test Circuit



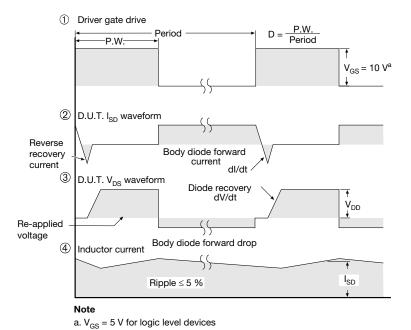


Fig. 19 - For N-Channel



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