

K4115-VB Datasheet

N-Channel 900V (D-S) Super Junction Power MOSFET

PRODUCT SUMMARY

| | | |
|------------------------------------|------------------------|------|
| V_{DS} (V) at T_J max. | 900 | |
| $R_{DS(on)}$ at 25 °C (Ω) | $V_{GS} = 10\text{ V}$ | 0.75 |
| Q_g max. (nC) | 20 | |
| Q_{gs} (nC) | 2.4 | |
| Q_{gd} (nC) | 11 | |
| Configuration | Single | |

FEATURES

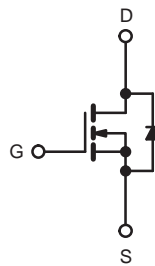
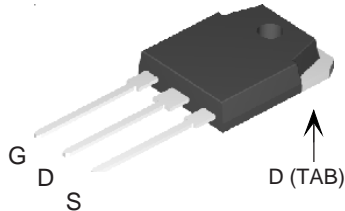
- Low figure-of-merit (FOM) $R_{DS(on)} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)



APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial

TO-3P



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ °C}$, unless otherwise noted)

| PARAMETER | | | SYMBOL | LIMIT | UNIT |
|---|-------------------------|-------------------------|-----------------------------------|-------------|------|
| Drain-Source Voltage | | | V _{DS} | 900 | V |
| Gate-Source Voltage | | | V _{GS} | ± 30 | |
| Continuous Drain Current (T _J = 150 °C) | V _{GS} at 10 V | T _C = 25 °C | I _D | 9 | A |
| | | T _C = 100 °C | | 7.3 | |
| Pulsed Drain Current ^a | | | I _{DM} | 28 | |
| Linear Derating Factor | | | | 1.89 | W/°C |
| Single Pulse Avalanche Energy ^b | | | E _{AS} | 86 | mJ |
| Maximum Power Dissipation | | | P _D | 109 | W |
| Operating Junction and Storage Temperature Range | | | T _J , T _{stg} | -55 to +150 | °C |
| Drain-Source Voltage Slope | T _J = 125 °C | | dV/dt | 50 | V/ns |
| Reverse Diode dV/dt ^d | | 3.2 | | | |
| Soldering Recommendations (Peak Temperature) ^c | for 10 s | | | 300 | °C |


Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ °C}$, $L = 28.2\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 3.5\text{ A}$.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, $dI/dt = 100\text{ A}/\mu\text{s}$, starting $T_J = 25\text{ °C}$.

THERMAL RESISTANCE RATINGS

| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
|----------------------------------|------------|------|------|------|
| Maximum Junction-to-Ambient | R_{thJA} | - | 72 | °C/W |
| Maximum Junction-to-Case (Drain) | R_{thJC} | - | 0.7 | |

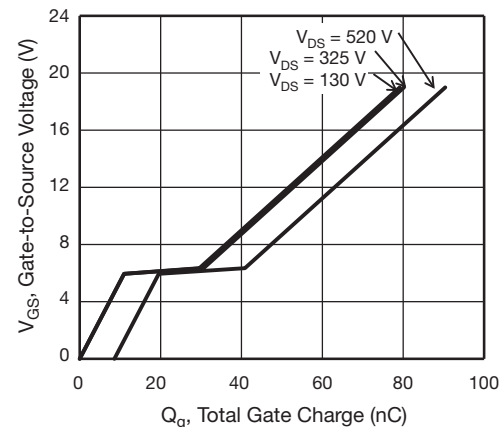
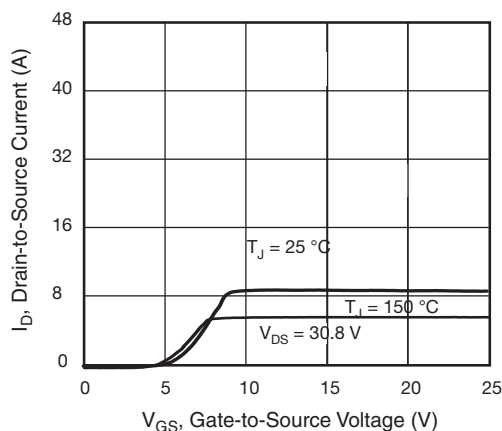
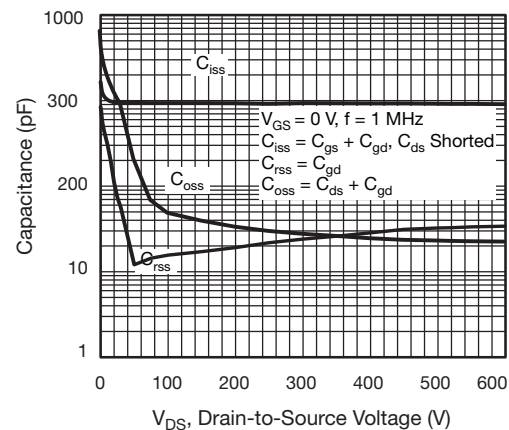
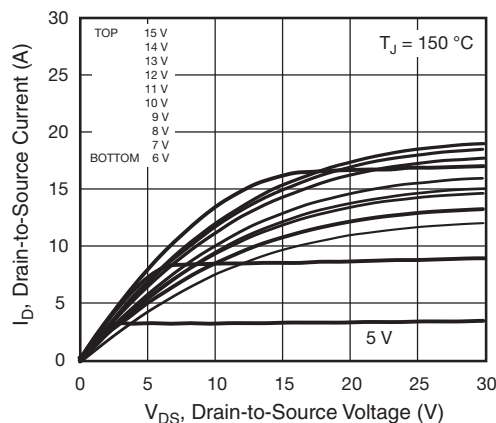
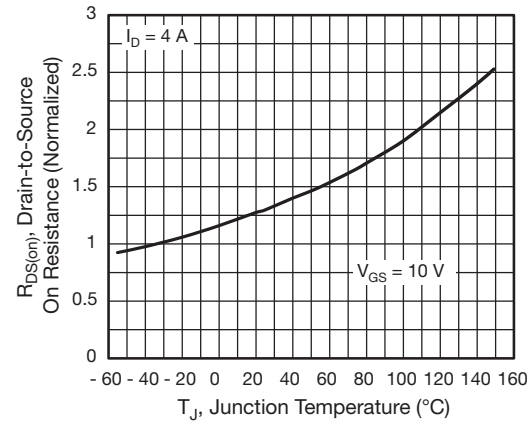
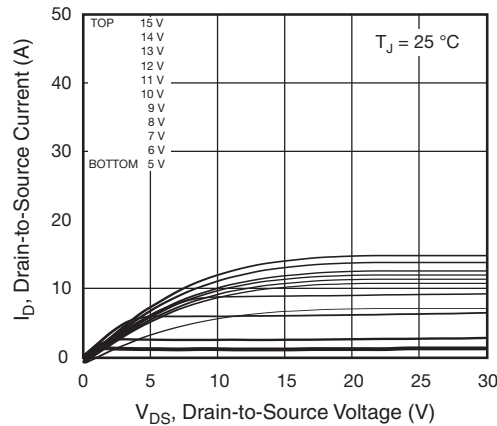
SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---------------------|--|---|------|------|-----------|---------------|
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | | 900 | - | - | V |
| V_{DS} Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to 25 °C, $I_D = 1\text{ mA}$ | | - | 0.65 | - | V/°C |
| Gate-Source Threshold Voltage (N) | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | | 2 | - | 4 | V |
| Gate-Source Leakage | I_{GSS} | $V_{GS} = \pm 20\text{ V}$ | | - | - | ± 100 | nA |
| | | $V_{GS} = \pm 30\text{ V}$ | | - | - | ± 1 | μA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 900\text{ V}, V_{GS} = 0\text{ V}$ | | - | - | 1 | μA |
| | | $V_{DS} = 620\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^{\circ}\text{C}$ | | - | - | 10 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$ | $I_D = 6\text{ A}$ | - | 0.75 | - | Ω |
| Forward Transconductance | g_{fs} | $V_{DS} = 30\text{ V}, I_D = 6\text{ A}$ | | - | 19 | - | S |
| Dynamic | | | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0\text{ V},$ $V_{DS} = 100\text{ V},$ $f = 1\text{ MHz}$ | | - | 373 | - | pF |
| Output Capacitance | C_{oss} | | | - | 26 | - | |
| Reverse Transfer Capacitance | C_{rss} | | | - | 14 | - | |
| Effective Output Capacitance, Energy Related ^a | $C_{O(er)}$ | $V_{DS} = 0\text{ V to } 520\text{ V}, V_{GS} = 0\text{ V}$ | | - | 46 | - | |
| Effective Output Capacitance, Time Related ^b | $C_{O(tr)}$ | | | - | 64 | - | |
| Total Gate Charge | Q_g | $V_{GS} = 10\text{ V}$ | $I_D = 6\text{ A}, V_{DS} = 520\text{ V}$ | - | 26 | - | nC |
| Gate-Source Charge | Q_{gs} | | | - | 2.1 | - | |
| Gate-Drain Charge | Q_{gd} | | | - | 2.8 | - | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 620\text{ V}, I_D = 6\text{ A},$ $V_{GS} = 10\text{ V}, R_g = 9.1\text{ }\Omega$ | | - | 26 | - | ns |
| Rise Time | t_r | | | - | 55.7 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | - | 71 | - | |
| Fall Time | t_f | | | - | 41 | - | |
| Gate Input Resistance | R_g | $f = 1\text{ MHz}, \text{open drain}$ | | - | 3.5 | - | Ω |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous Source-Drain Diode Current | I_S | MOSFET symbol showing the integral reverse p - n junction diode  | | - | - | 7 | A |
| Pulsed Diode Forward Current | I_{SM} | | | - | - | 18 | |
| Diode Forward Voltage | V_{SD} | $T_J = 25\text{ }^{\circ}\text{C}, I_S = 6\text{ A}, V_{GS} = 0\text{ V}$ | | - | - | 1.4 | V |
| Reverse Recovery Time | t_{rr} | $T_J = 25\text{ }^{\circ}\text{C}, I_F = I_S = 6\text{ A},$ $dI/dt = 100\text{ A}/\mu\text{s}, V_R = 400\text{ V}$ | | - | 192 | - | ns |
| Reverse Recovery Charge | Q_{rr} | | | - | 2.4 | - | μC |
| Reverse Recovery Current | I_{RRM} | | | - | 11 | - | A |

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
 b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



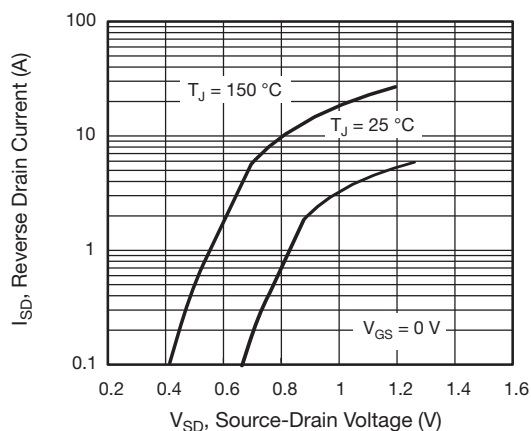


Fig. 7 - Typical Source-Drain Diode Forward Voltage

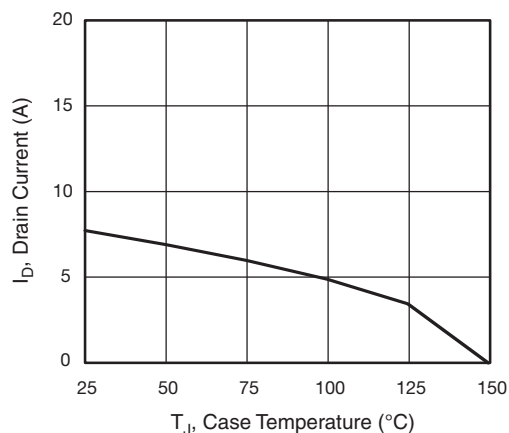


Fig. 9 - Maximum Drain Current vs. Case Temperature

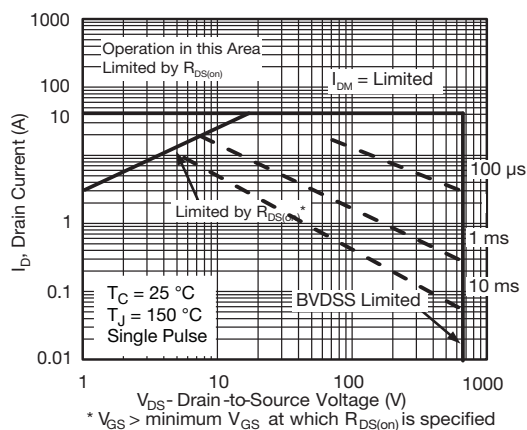


Fig. 8 - Maximum Safe Operating Area

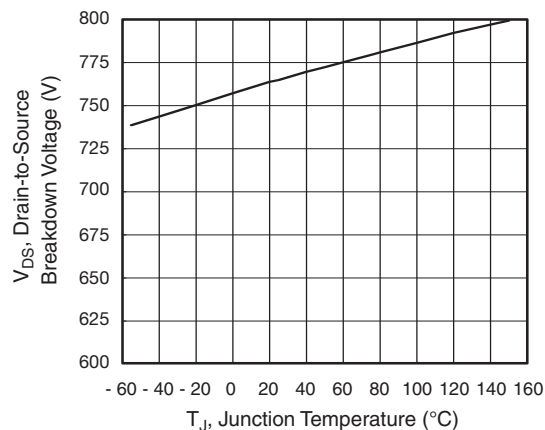


Fig. 10 - Temperature vs. Drain-to-Source Voltage

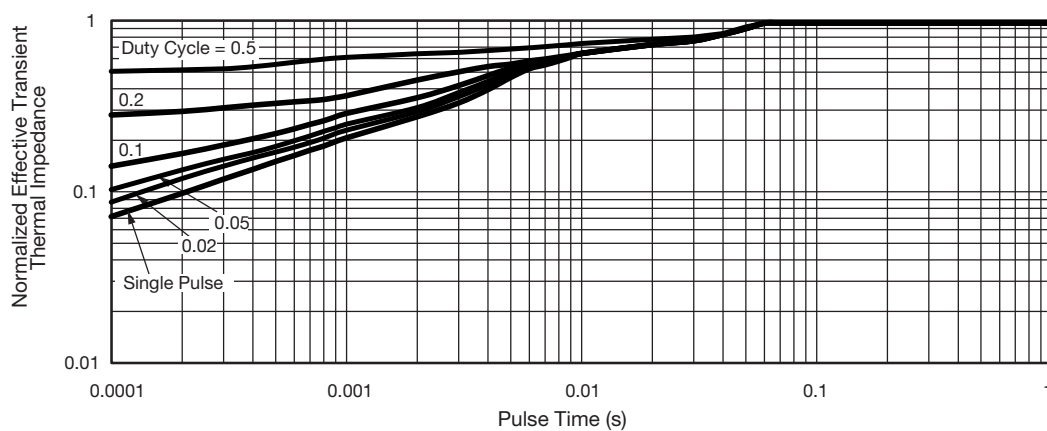


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

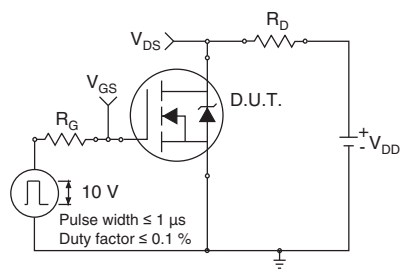


Fig. 12 - Switching Time Test Circuit

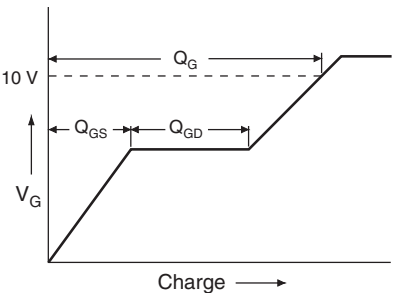


Fig. 16 - Basic Gate Charge Waveform

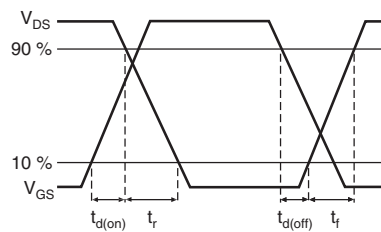


Fig. 13 - Switching Time Waveforms

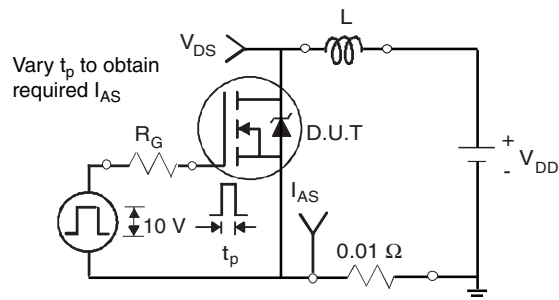


Fig. 14 - Unclamped Inductive Test Circuit

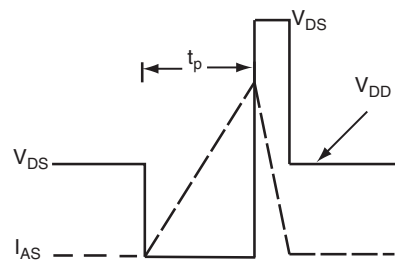


Fig. 15 - Unclamped Inductive Waveforms

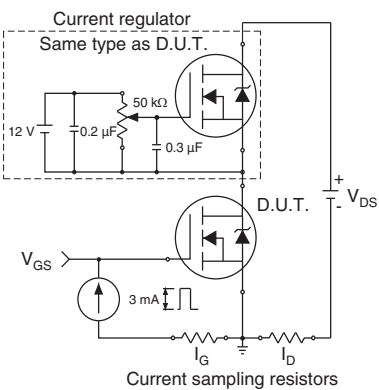
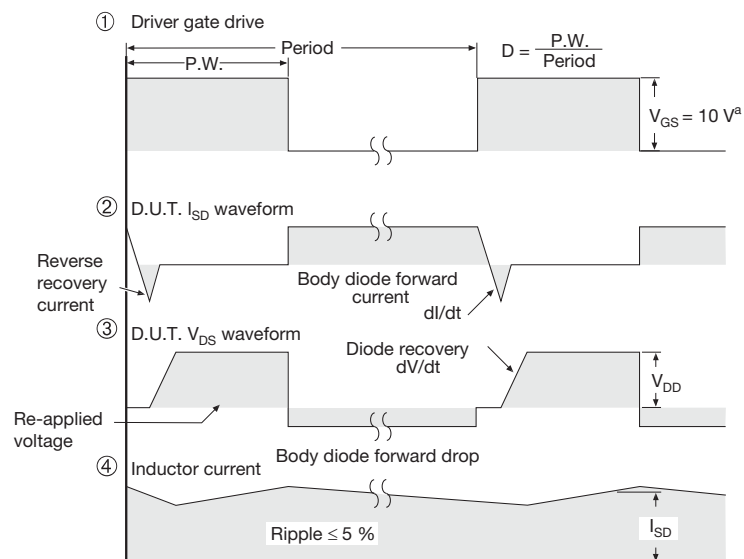
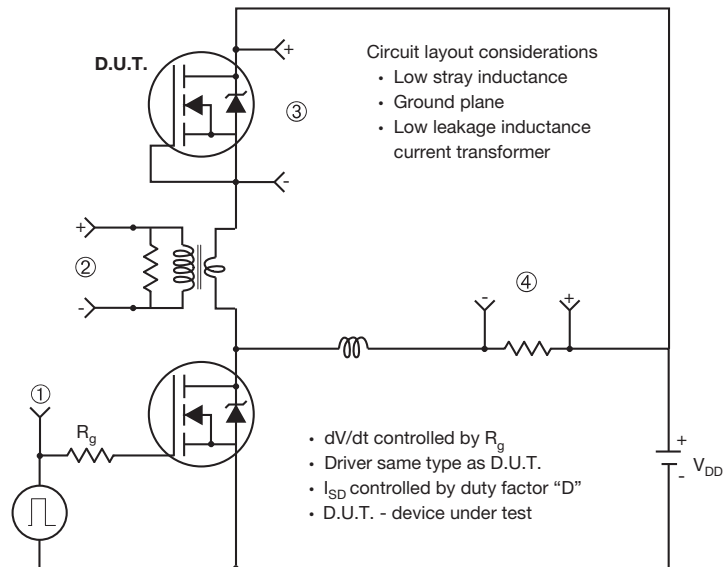


Fig. 17 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 18 - For N-Channel

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