

K1162-VB Datasheet

N-Channel 600V (D-S) Super Junction MOSFET



| PRODUCT SUMMARY | | |
|------------------------------------|-----------------|------|
| V_{DS} (V) at T_J max. | 650 | |
| $R_{DS(on)}$ at 25 °C (Ω) | $V_{GS} = 10$ V | 0.38 |
| Q_g max. (nC) | 38 | |
| Q_{gs} (nC) | 4 | |
| Q_{gd} (nC) | 4.2 | |
| Configuration | Single | |

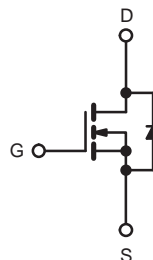
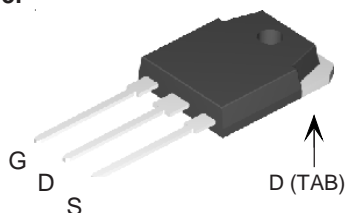
FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial

TO-3P



N-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted) | | | | | |
|---|-------------------------|-------------------------|-----------------------------------|--------------|------|
| PARAMETER | | | SYMBOL | LIMIT | UNIT |
| Drain-Source Voltage | | | V _{DS} | 600 | V |
| Gate-Source Voltage | | | V _{GS} | ± 30 | |
| Continuous Drain Current (T _J = 150 °C) | V _{GS} at 10 V | T _C = 25 °C | I _D | 11 | A |
| | | T _C = 100 °C | | 9.7 | |
| Pulsed Drain Current ^a | | | I _{DM} | 50 | |
| Linear Derating Factor | | | | 1.67/1.5/0.3 | W/°C |
| Single Pulse Avalanche Energy ^b | | | E _{AS} | 132 | mJ |
| Maximum Power Dissipation | | | P _D | 83/83/31 | W |
| Operating Junction and Storage Temperature Range | | | T _J , T _{stg} | -55 to +150 | °C |
| Drain-Source Voltage Slope | T _J = 125 °C | | dV/dt | 50 | V/ns |
| Reverse Diode dV/dt ^d | | | | 3.1 | |
| Soldering Recommendations (Peak Temperature) ^c | for 10 s | | | 300 | °C |

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 4.5$ A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C.

THERMAL RESISTANCE RATINGS

| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
|----------------------------------|------------|------|------|------|
| Maximum Junction-to-Ambient | R_{thJA} | - | 60 | °C/W |
| Maximum Junction-to-Case (Drain) | R_{thJC} | - | 0.6 | |

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|----------------------------------|--|---|------|------|-------|------|
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | V _{DS} | V _{GS} = 0 V, I _D = 250 μA | | 600 | - | - | V |
| V _{DS} Temperature Coefficient | ΔV _{DS} /T _J | Reference to 25 °C, I _D = 1 mA | | - | 0.65 | - | V/°C |
| Gate-Source Threshold Voltage (N) | V _{GS(th)} | V _{DS} = V _{GS} , I _D = 250 μA | | 2 | - | 4 | V |
| Gate-Source Leakage | I _{GSS} | V _{GS} = ± 20 V | | - | - | ± 100 | nA |
| | | V _{GS} = ± 30 V | | - | - | ± 1 | μA |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} = 650 V, V _{GS} = 0 V | | - | - | 1 | μA |
| | | V _{DS} = 520 V, V _{GS} = 0 V, T _J = 125 °C | | - | - | 10 | |
| Drain-Source On-State Resistance | R _{DS(on)} | V _{GS} = 10 V | I _D = 5 A | - | 0.38 | - | Ω |
| Forward Transconductance | g _{fs} | V _{DS} = 30 V, I _D = 5 A | | - | 16 | - | S |
| Dynamic | | | | | | | |
| Input Capacitance | C _{iss} | V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz | | - | 680 | - | pF |
| Output Capacitance | C _{oss} | | | - | 140 | - | |
| Reverse Transfer Capacitance | C _{rss} | | | - | 5 | - | |
| Effective Output Capacitance, Energy Related ^a | C _{o(er)} | V _{DS} = 0 V to 520 V, V _{GS} = 0 V | | - | 63 | - | pF |
| Effective Output Capacitance, Time Related ^b | C _{o(tr)} | | | - | 113 | - | |
| Total Gate Charge | Q _g | V _{GS} = 10 V | I _D = 5 A, V _{DS} = 520 V | - | 38 | 56 | nC |
| Gate-Source Charge | Q _{gs} | | | - | 4 | - | |
| Gate-Drain Charge | Q _{gd} | | | - | 4.5 | - | |
| Turn-On Delay Time | t _{d(on)} | V _{DD} = 520 V, I _D = 5 A, V _{GS} = 10 V, R _g = 9.1 Ω | | - | 13 | 25 | ns |
| Rise Time | t _r | | | - | 11 | 35 | |
| Turn-Off Delay Time | t _{d(off)} | | | - | 81 | 90 | |
| Fall Time | t _f | | | - | 25 | 40 | |
| Gate Input Resistance | R _g | f = 1 MHz, open drain | | - | 3.5 | - | Ω |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous Source-Drain Diode Current | I _S | MOSFET symbol showing the integral reverse p - n junction diode  | | - | - | 11 | A |
| Pulsed Diode Forward Current | I _{SM} | | | - | - | 55 | |
| Diode Forward Voltage | V _{SD} | T _J = 25 °C, I _S = 5 A, V _{GS} = 0 V | | - | - | 1.5 | V |
| Reverse Recovery Time | t _{rr} | T _J = 25 °C, I _F = I _S = 5 A, di/dt = 100 A/μs, V _R = 400 V | | - | 270 | - | ns |
| Reverse Recovery Charge | Q _{rr} | | | - | 3.3 | - | μC |
| Reverse Recovery Current | I _{RRM} | | | - | 30 | - | A |

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
 b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



Fig. 7 - Typical Source-Drain Diode Forward Voltage



Fig. 9 - Maximum Drain Current vs. Case Temperature



Fig. 8 - Maximum Safe Operating Area



Fig. 10 - Temperature vs. Drain-to-Source Voltage

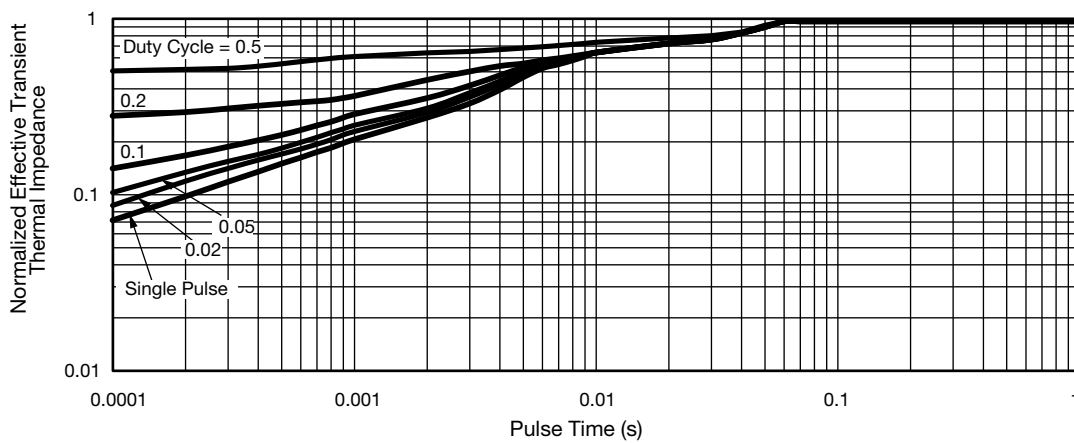


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case



Fig. 12 - Switching Time Test Circuit



Fig. 16 - Basic Gate Charge Waveform



Fig. 13 - Switching Time Waveforms



Fig. 14 - Unclamped Inductive Test Circuit



Fig. 15 - Unclamped Inductive Waveforms



Fig. 17 - Gate Charge Test Circuit

**Note**

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 18 - For N-Channel

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