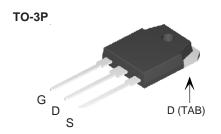


# IXTQ50N20P-VB Datasheet N-Channel 200-V (D-S) MOSFET

PRODUCT SUMMARY				
V <sub>(BR)DSS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)	
200	0.048 at V <sub>GS</sub> = 15 V	60	57	
200	0.046 at V <sub>GS</sub> = 10 V	55	57	



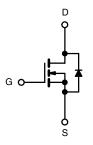
### **FEATURES**

- Trench Power MOSFETS
- 175 °C Junction Temperature
- 100 % R<sub>g</sub> and UIS Tested



### **APPLICATIONS**

- Power Supply
- Lighting Systems



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	T <sub>A</sub> = 25 °C, unless oth	erwise noted			
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V <sub>DS</sub>	200	V		
Gate-Source Voltage		V <sub>GS</sub>	± 25	V	
Continuous Drain Current (T <sub>.I</sub> = 175 °C)	T <sub>C</sub> = 25 °C	I-	60		
Continuous Diain Current (1) = 173 C)	T <sub>C</sub> = 100 °C	I <sub>D</sub>	40		
Pulsed Drain Current		I <sub>DM</sub>	180	Α	
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	20		
Single Pulse Avalanche Energy <sup>a</sup>	L = 0.111111	E <sub>AS</sub>	20	mJ	
Maximum Power Dissipation <sup>a</sup>	T <sub>C</sub> = 25 °C	В	166 <sup>b</sup>	W	
	T <sub>A</sub> = 25 °C <sup>c</sup>	$ P_{D}$	3.12		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Limit	Unit	
Junction-to-Ambient (PCB Mount) <sup>c</sup>	R <sub>thJA</sub>	40	°C/W	
Junction-to-Case (Drain)	R <sub>thJC</sub>	0.75	10/00	

### Notes:

- a. Duty cycle  $\leq$  1 %.
- b. See SOA curve for voltage derating.
- c. When Mounted on 1" square PCB (FR-4 material).

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	200			- v
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2.5		4.5	
Gate-Body Leakage		$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 25 \text{ V}$			± 300	
Zero Gate Voltage Drain Current		V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V			1	μΑ
	I <sub>DSS</sub>	$V_{DS} = 200 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 100 ^{\circ}\text{C}$			25	
		$V_{DS} = 200 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 150 ^{\circ}\text{C}$			250	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	40			Α
Drain-Source On-State Resistance <sup>a</sup>		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		0.048		
		V <sub>GS</sub> = 15 V, I <sub>D</sub> = 20 A		0.046		Ω
	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 100 °C		0.088		
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 150 °C		0.120		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A	25			S
Dynamie <sup>tb</sup>						
Input Capacitance	C <sub>iss</sub>			3100		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz		300		
Reverse Transfer Capacitance	C <sub>rss</sub>			135		
T O	Q <sub>g</sub>	$V_{DS} = 100 \text{ V}, V_{GS} = 15 \text{ V}, I_D = 50 \text{ A}$		85	127	
Total Gate Charge <sup>c</sup>				57	85	20
Gate-Source Charge <sup>c</sup>	$Q_{gs}$	$V_{DS} = 100 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 50 \text{ A}$		14		nC
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			20		
Gate Resistance	$R_{g}$	f = 1 MHz		1.2	1.8	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			16	25	ns ns
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD}$ = 100 V, $R_L$ = 2 $\Omega$		170	260	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	$I_D \cong 50 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		27	42	
Fall Time <sup>c</sup>	t <sub>f</sub>			9	18	
Source Drain Diore Harings Sanar Cha	<b>Pagrépréstég</b> st]					
Continuous Current	I <sub>S</sub>				36	А
Pulsed Current	I <sub>SM</sub>				80	
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = 20 A, V <sub>GS</sub> = 0 V		0.86	1.5	٧
Reverse Recovery Time	t <sub>rr</sub>			116	175	ns
Peak Reverse Recovery Current	I <sub>RM(REC)</sub>			9	14	Α
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> = 40 A, di/dt = 100 A/μs		0.53	0.8	μC
Reverse Recovery Fall Time	t <sub>a</sub>	· '		84		•
Reverse Recovery Rise Time	t <sub>b</sub>			32		nS

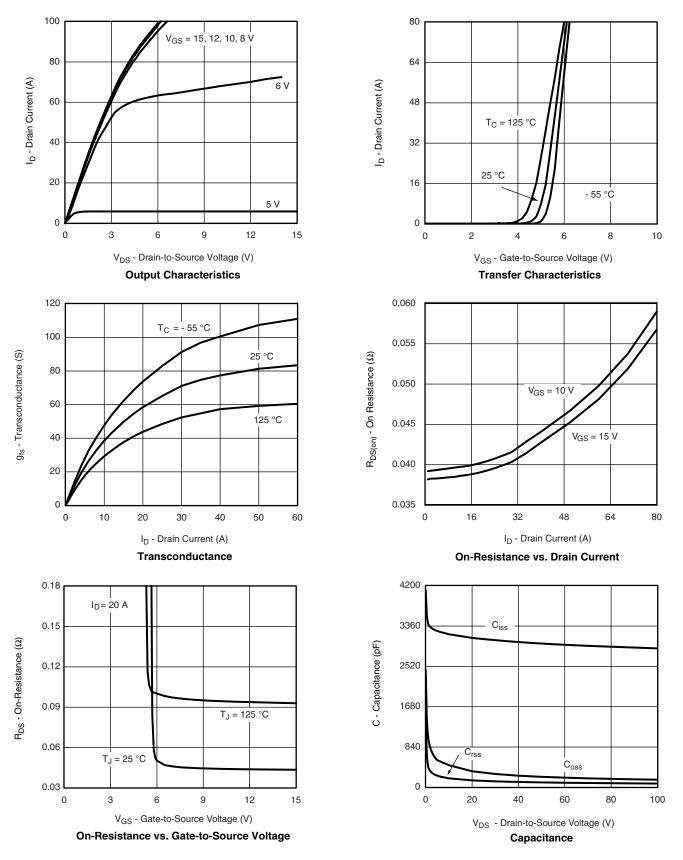
#### Notes:

- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

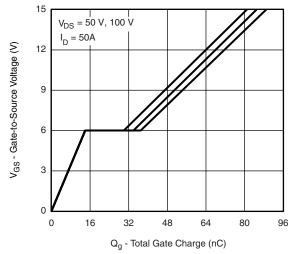


## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

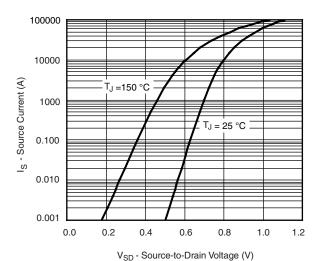




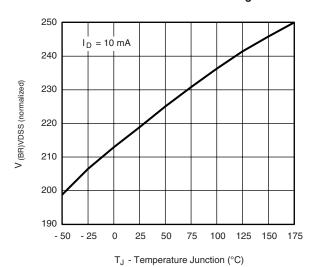
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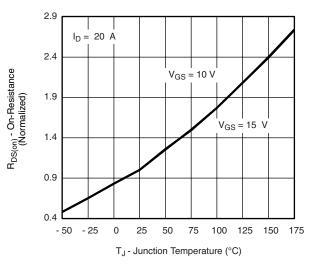




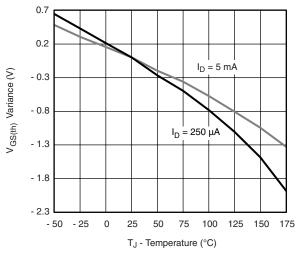
Source-Drain Diode Forward Voltage



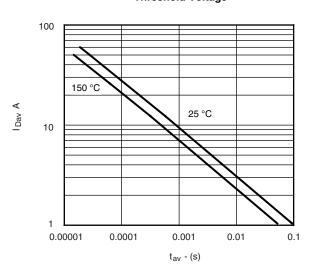
Drain Source Breakdown vs. Junction Temperature



#### On-Resistance vs. Junction Temperature



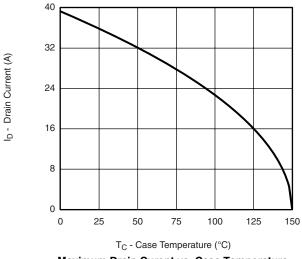
Threshold Voltage

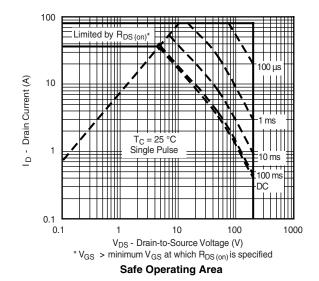


Single Pulse Avalanche Current Capability vs. Time

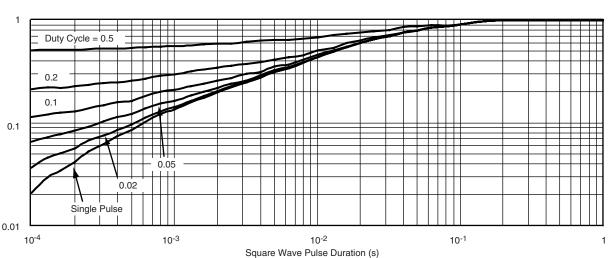


#### **THERMAL RATINGS**





**Maximum Drain Curent vs. Case Temperature** 



Normalized Thermal Transient Impedance, Junction-to-Case

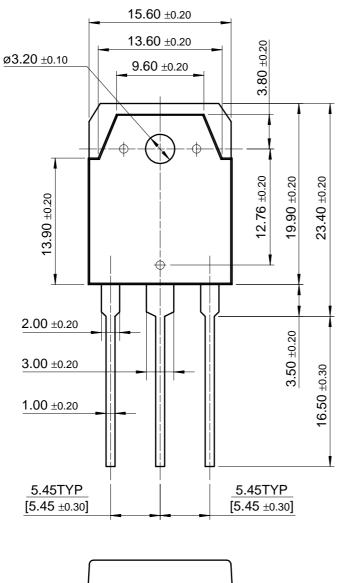
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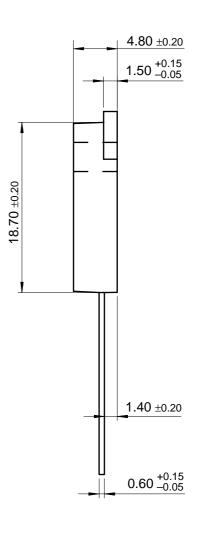
Normalized Effective Transient Thermal Impedance

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