

HY3215PM-VB Datasheet

N-Channel 150V (D-S) MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
150	0.017 at $V_{GS} = 10$ V	90 ^a

FEATURES

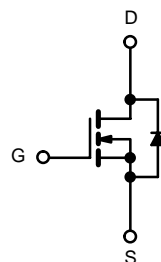
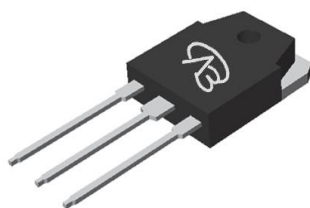
- Trench Power MOSFET
- 175 °C Junction Temperature
- Low Thermal Resistance Package
- 100 % R_g Tested


RoHS
 COMPLIANT

APPLICATIONS

- Isolated DC/DC Converters

TO-3P



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	150	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 175$ °C)	I_D	90 ^a	A
		75 ^a	
Pulsed Drain Current	I_{DM}	250	
Avalanche Current	I_{AS}	35	
Single Pulse Avalanche Energy ^b	E_{AS}	61	mJ
Maximum Power Dissipation ^b	P_D	375 ^c	W
		3.75	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient	R_{thJA}	40	°C/W
Junction-to-Case (Drain)	R_{thJC}	0.4	

Notes:

a. Package limited.

 b. Duty cycle ≤ 1 %.

c. See SOA curve for voltage derating.

d. When Mounted on 1" square PCB (FR-4 material).

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{DS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	150			V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1		4	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^{\circ}\text{C}$			50	
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, T_J = 175\text{ }^{\circ}\text{C}$			250	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	120			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}$		0.017		Ω
		$V_{GS} = 10\text{ V}, I_D = 30\text{ A}, T_J = 125\text{ }^{\circ}\text{C}$		0.023		
		$V_{GS} = 10\text{ V}, I_D = 30\text{ A}, T_J = 175\text{ }^{\circ}\text{C}$		0.034		
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 30\text{ A}$	25			S
Dynamic ^b						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		5100		pF
Output Capacitance	C_{oss}			480		
Reverse Transfer Capacitance	C_{rss}			210		
Total Gate Charge ^c	Q_g	$V_{DS} = 100\text{ V}, V_{GS} = 10\text{ V}, I_D = 65\text{ A}$		90	130	nC
Gate-Source Charge ^c	Q_{gs}			23		
Gate-Drain Charge ^c	Q_{gd}			34		
Gate Resistance	R_g		0.5	1.7	3.3	Ω
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 100\text{ V}, R_L = 1.5\text{ }\Omega$ $I_D \cong 65\text{ A}, V_{GEN} = 10\text{ V}, R_g = 2.5\text{ }\Omega$		24	35	ns
Rise Time ^c	t_r			220	330	
Turn-Off Delay Time ^c	$t_{d(off)}$			45	70	
Fall Time ^c	t_f			200	300	
Source-Drain Diode Ratings and Characteristics $T_C = 25\text{ }^{\circ}\text{C}$ ^b						
Continuous Current	I_S				65	A
Pulsed Current	I_{SM}				140	
Forward Voltage ^a	V_{SD}	$I_F = 65\text{ A}, V_{GS} = 0\text{ V}$		1.0	1.5	V
Reverse Recovery Time	t_{rr}	$I_F = 50\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		130	200	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			8	12	A
Reverse Recovery Charge	Q_{rr}			0.52	1.2	μC

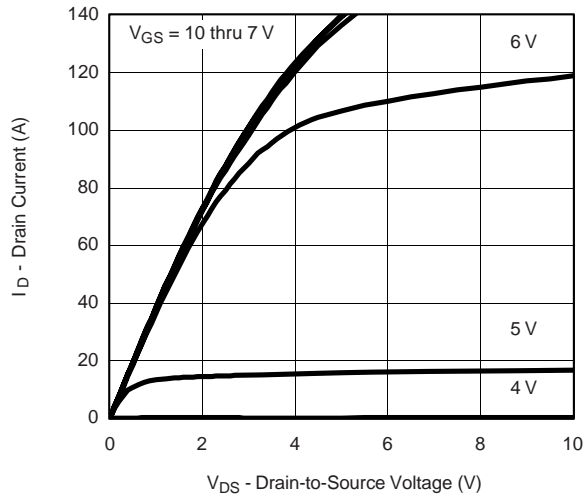
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

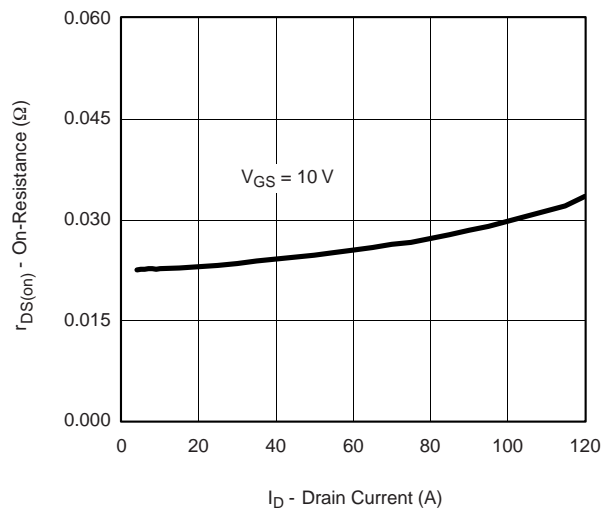
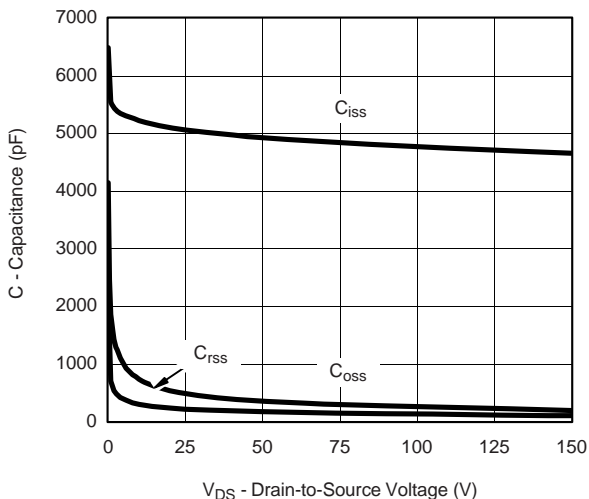
b. Guaranteed by design, not subject to production testing.

c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Output Characteristics

Transfer Characteristics

Transconductance

On-Resistance vs. Drain Current

Capacitance

Gate Charge

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

On-Resistance vs. Junction Temperature

Source-Drain Diode Forward Voltage

Avalanche Current vs. Time

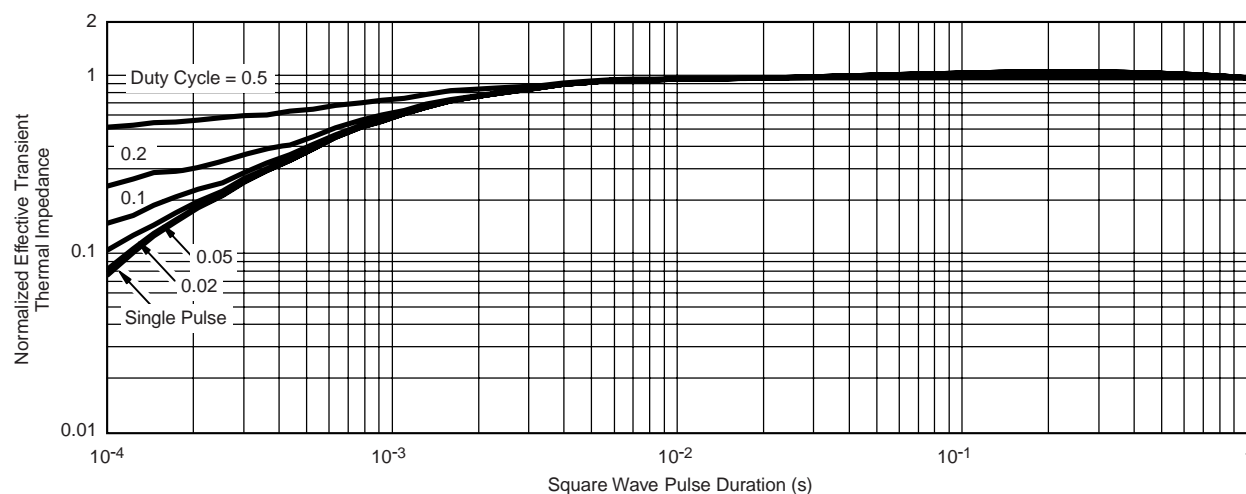
Drain Source Breakdown vs. Junction Temperature

The graph shows the relationship between Drain Current (I_D) and Ambient Temperature (T_C) for the 2N3866 JFET. The current is constant at approximately 65 mA from 0°C to 25°C, then decreases to 0 mA at 175°C.

T_C - Ambient Temperature ($^{\circ}\text{C}$)	I_D - Drain Current (mA)
0	65
25	65
50	60
75	55
100	45
125	35
150	25
175	0

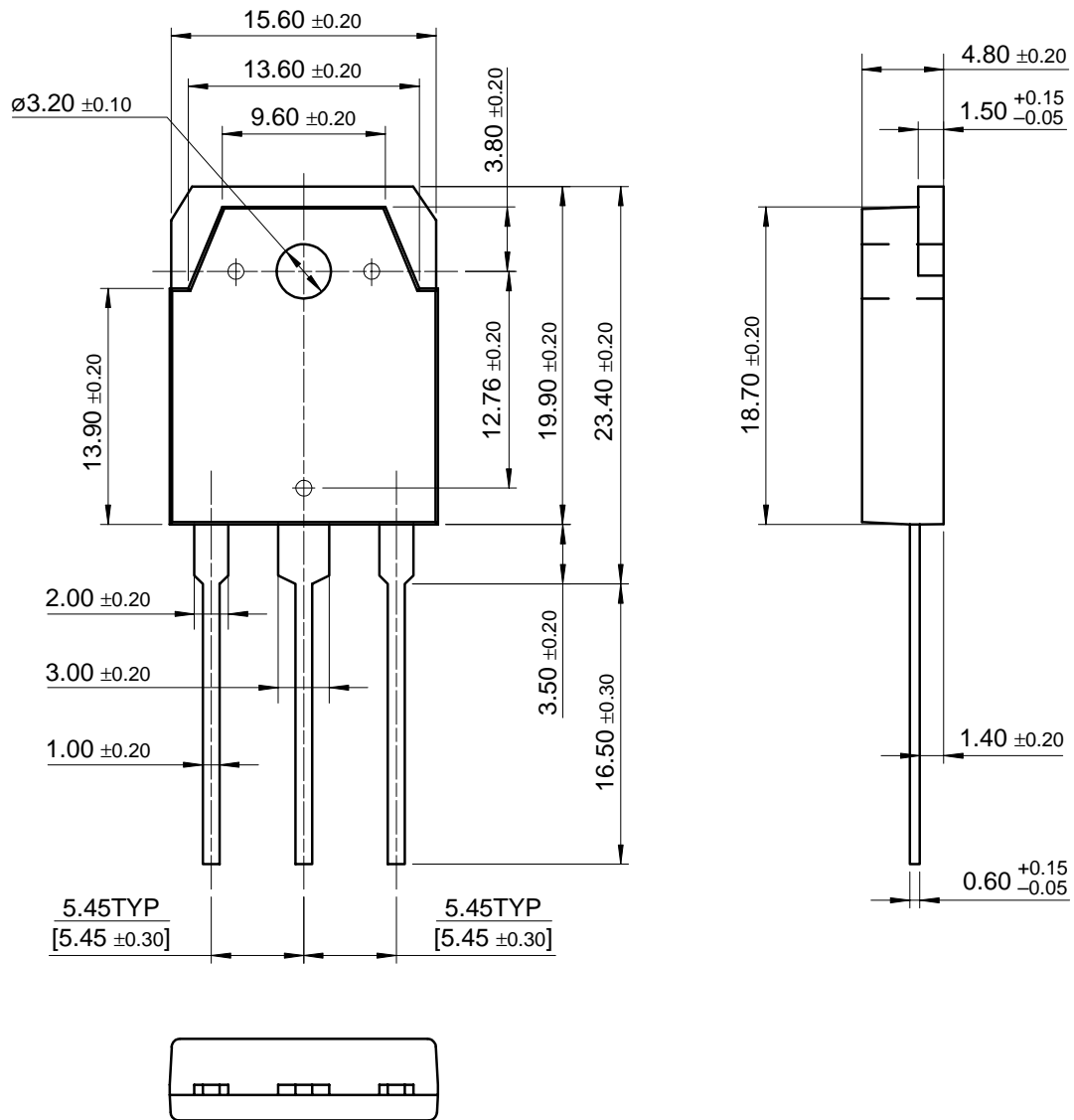
Figure 10 is a log-log plot showing the Pulsed Load Regulation Characteristics. The Y-axis represents Drain Current (I_D) in Amperes (A), ranging from 0.1 to 1000. The X-axis represents Drain-to-Source Voltage (V_{DS}) in Volts (V), ranging from 0.1 to 1000. The plot shows the relationship between I_D and V_{DS} for various pulse widths: 10 μ s, 100 μ s, 1 ms, 10 ms, 100 ms, and DC. A horizontal line at $I_D \approx 60$ A is labeled $r_{DS(on)}$ Limited*. The curves show that I_D increases with V_{DS} for short pulses and decreases for longer pulses. The temperature is specified as $T_C = 25^\circ\text{C}$ and the test condition is a Single Pulse.

Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

TO-3P



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