

FPS43N50K-VB Datasheet

N-Channel 600V(D-S) Super Junction Power MOSFET

PRODUCT SUMMARY

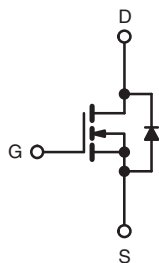
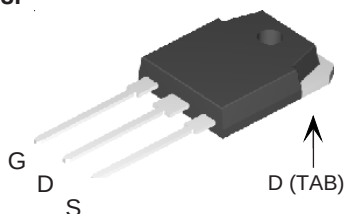
V_{DS} (V) at T_J max.	600	
$R_{DS(on)}$ at 25 °C (Ω)	$V_{GS} = 10$ V	0.06
Q_g max. (nC)	273	
Q_{gs} (nC)	46	
Q_{gd} (nC)	79	
Configuration	Single	

FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)


RoHS
 COMPLIANT

TO-3P



N-Channel MOSFET

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Renewable energy
 - Solar (PV inverters)

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	600	V
Gate-Source Voltage			V _{GS}	± 30	
Continuous Drain Current (T _J = 150 °C)	V _{GS} at 10 V	T _C = 25 °C	I _D	47	A
		T _C = 100 °C		30	
Pulsed Drain Current ^a			I _{DM}	142	
Linear Derating Factor				3.3	W/°C
Single Pulse Avalanche Energy ^b			E _{AS}	1410	mJ
Maximum Power Dissipation			P _D	415	W
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +150	°C
Drain-Source Voltage Slope	T _J = 125 °C		dV/dt	37	V/ns
Reverse Diode dV/dt ^d				9	
Soldering Recommendations (Peak Temperature) ^c	for 10 s			300	°C

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DS} = 50$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 10$ A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.3	

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		600	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.70	-	V/°C
Gate-Source Threshold Voltage (N)	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2	-	4	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
		V _{GS} = ± 30 V		-	-	± 1	μA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 650 V, V _{GS} = 0 V		-	-	1	μA
		V _{DS} = 520 V, V _{GS} = 0 V, T _J = 125 °C		-	-	25	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 24 A	-	0.06	-	Ω
Forward Transconductance	g _{fs}	V _{DS} = 30 V, I _D = 24 A		-	16.7	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz		-	5682	-	pF
Output Capacitance	C _{oss}			-	251	-	
Reverse Transfer Capacitance	C _{rss}			-	1	-	
Effective Output Capacitance, Energy Related ^a	C _{o(er)}	V _{DS} = 0 V to 520 V, V _{GS} = 0 V		-	192	-	
Effective Output Capacitance, Time Related ^b	C _{o(tr)}			-	665	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 24 A, V _{DS} = 520 V	-	182	273	nC
Gate-Source Charge	Q _{gs}			-	46	-	
Gate-Drain Charge	Q _{gd}			-	79	-	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 520 V, I _D = 6 A, V _{GS} = 10 V, R _g = 9.1 Ω		-	47	94	ns
Rise Time	t _r			-	87	131	
Turn-Off Delay Time	t _{d(off)}			-	156	234	
Fall Time	t _f			-	103	206	
Gate Input Resistance	R _g	f = 1 MHz, open drain		-	0.64	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	47	A
Pulsed Diode Forward Current	I _{SM}			-	-	139	
Diode Forward Voltage	V _{SD}	T _J = 25 °C, I _S = 24 A, V _{GS} = 0 V		-	0.9	1.2	V
Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = I _S = 24 A, di/dt = 100 A/μs, V _R = 25 V		-	753	1506	ns
Reverse Recovery Charge	Q _{rr}			-	14	28	μC
Reverse Recovery Current	I _{RRM}			-	28	-	A

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
 b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

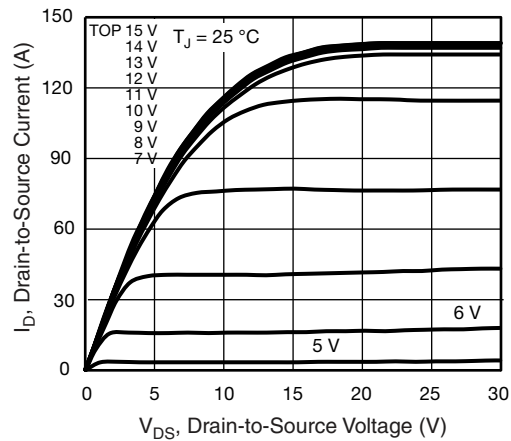


Fig. 1 - Typical Output Characteristics

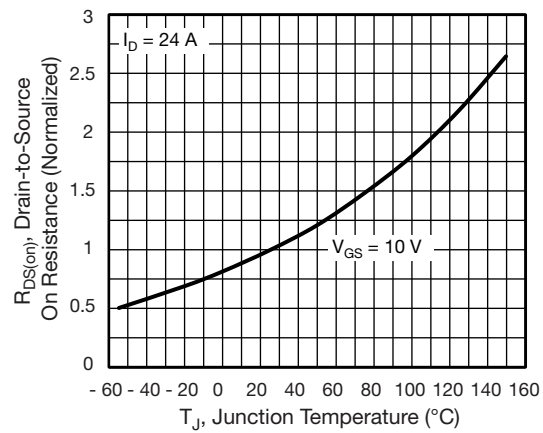


Fig. 4 - Normalized On-Resistance vs. Temperature

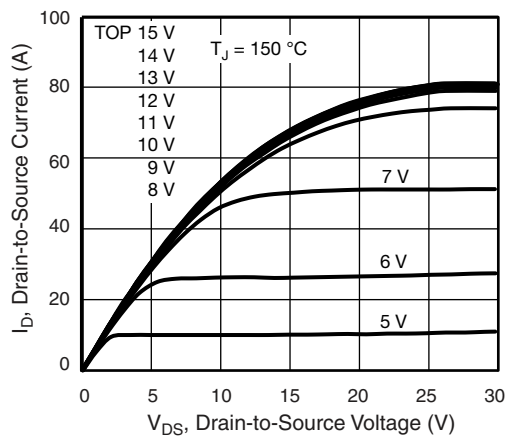


Fig. 2 - Typical Output Characteristics

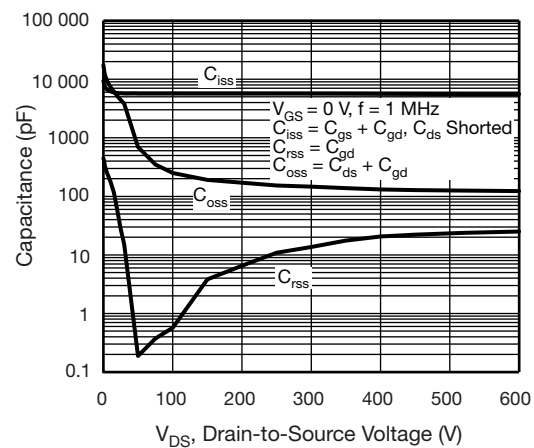


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

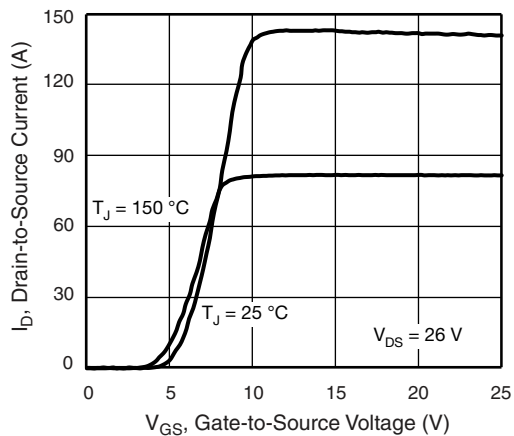


Fig. 3 - Typical Transfer Characteristics

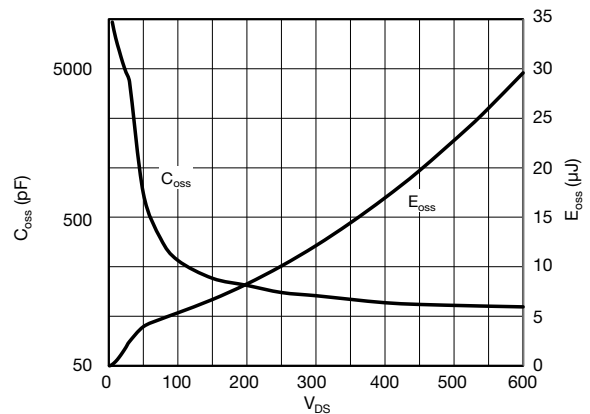


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

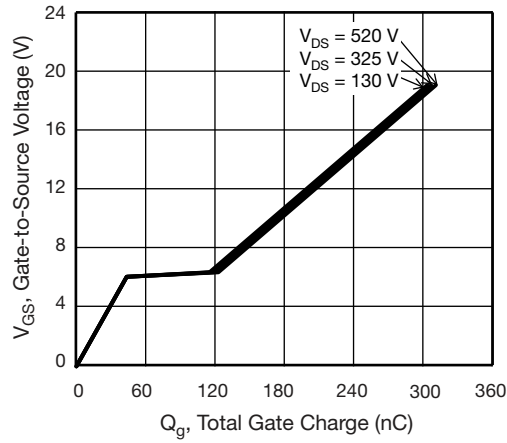


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

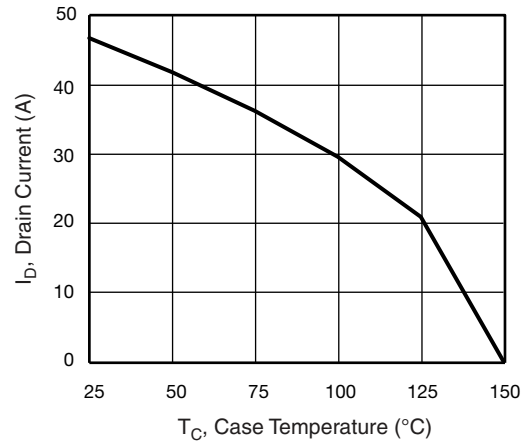


Fig. 10 - Maximum Drain Current vs. Case Temperature

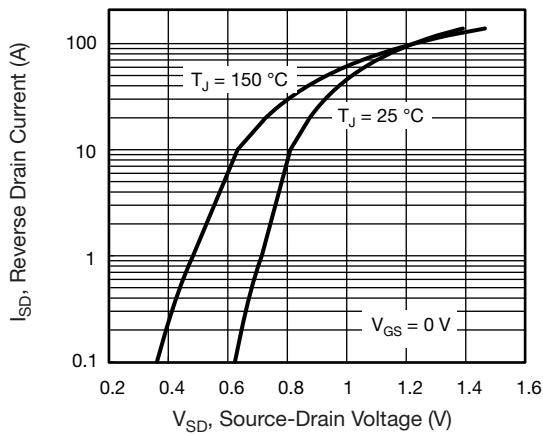


Fig. 8 - Typical Source-Drain Diode Forward Voltage

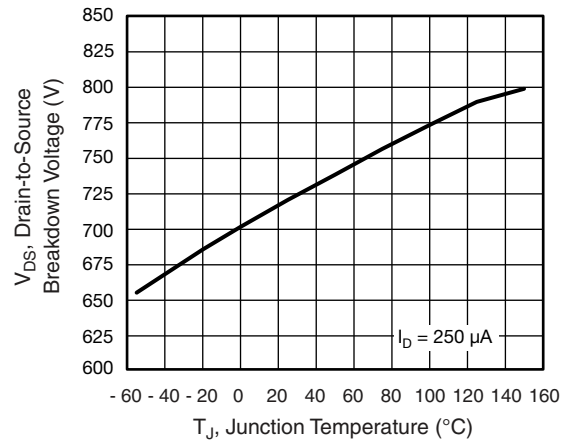


Fig. 11 - Temperature vs. Drain-to-Source Voltage

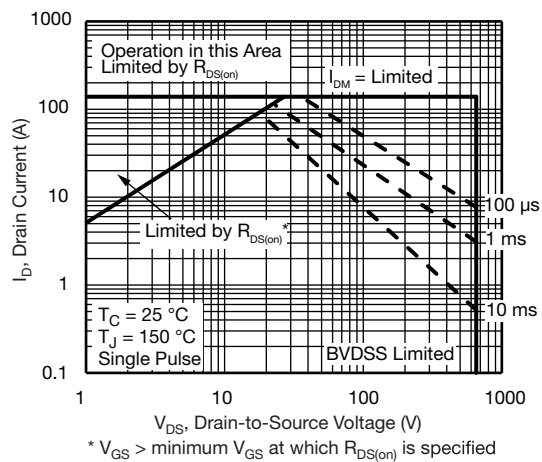


Fig. 9 - Maximum Safe Operating Area

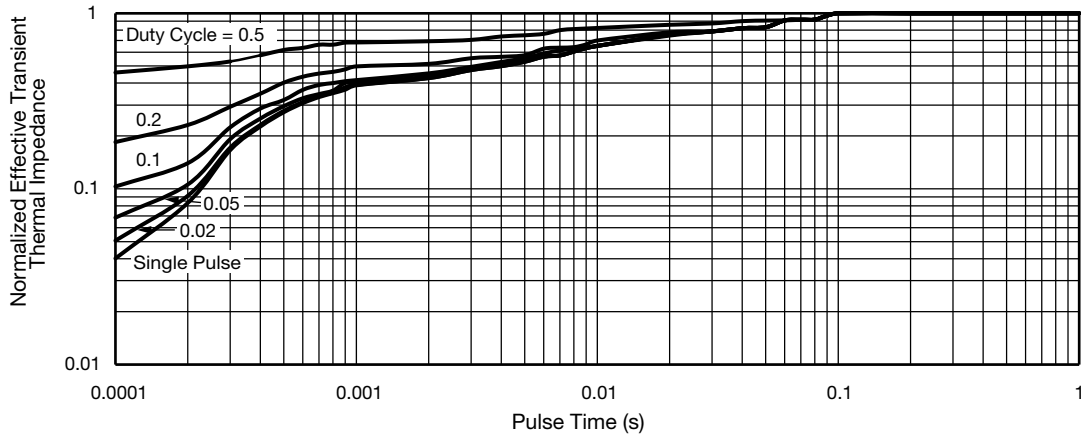


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

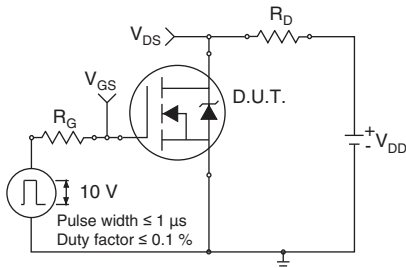


Fig. 13 - Switching Time Test Circuit

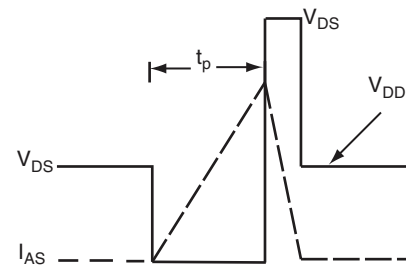


Fig. 16 - Unclamped Inductive Waveforms

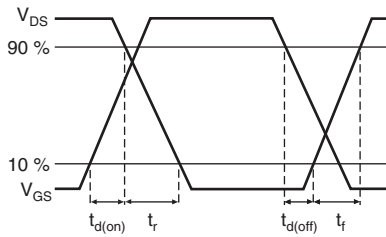


Fig. 14 - Switching Time Waveforms

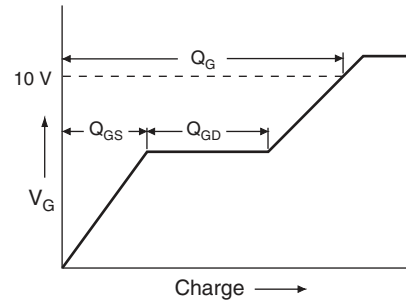


Fig. 17 - Basic Gate Charge Waveform

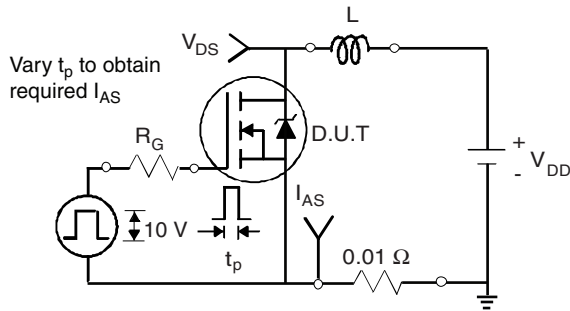


Fig. 15 - Unclamped Inductive Test Circuit

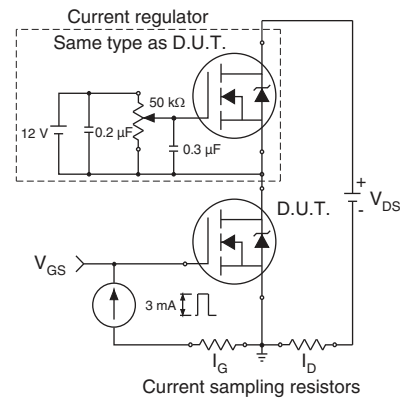
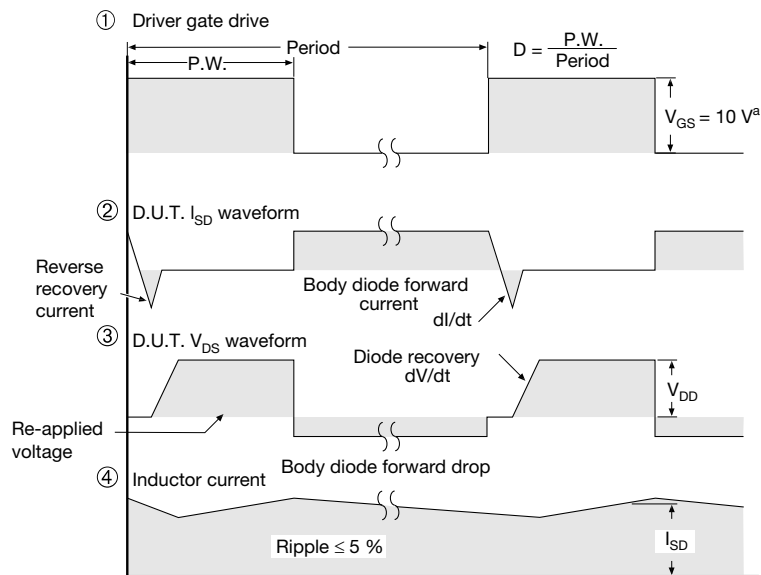
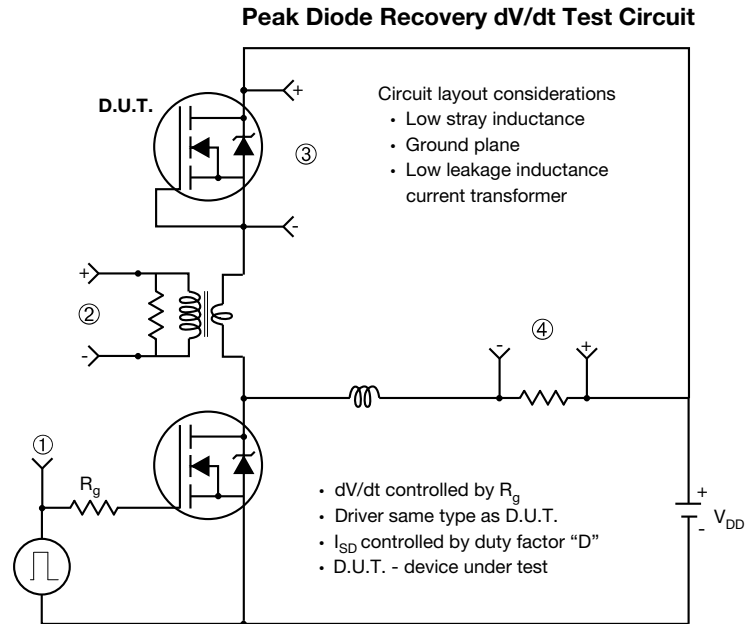


Fig. 18 - Gate Charge Test Circuit

**Note**a. $V_{GS} = 5\text{ V}$ for logic level devices**Fig. 19 - For N-Channel**

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