

2SK2606-VB Datasheet

N-Channel 900V (D-S) Super Junction Power MOSFET

PRODUCT SUMMARY

| | | |
|------------------------------------|------------------------|------|
| V_{DS} (V) at T_J max. | 900 | |
| $R_{DS(on)}$ at 25 °C (Ω) | $V_{GS} = 10\text{ V}$ | 0.75 |
| Q_g max. (nC) | 20 | |
| Q_{gs} (nC) | 2.4 | |
| Q_{gd} (nC) | 11 | |
| Configuration | Single | |

FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)

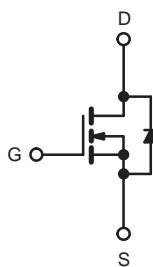
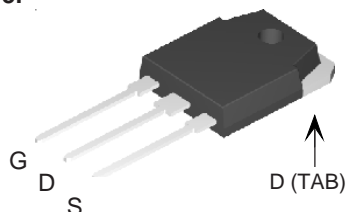


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APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial

TO-3P



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ °C}$, unless otherwise noted)

| PARAMETER | | | SYMBOL | LIMIT | UNIT |
|--|-------------------------------------|-------------------------------------|----------------|-------------|-----------------------|
| Drain-Source Voltage | | | V_{DS} | 900 | V |
| Gate-Source Voltage | | | V_{GS} | ± 30 | |
| Continuous Drain Current ($T_J = 150\text{ }^{\circ}\text{C}$) | V_{GS} at 10 V | $T_C = 25\text{ }^{\circ}\text{C}$ | I_D | 9 | A |
| | | $T_C = 100\text{ }^{\circ}\text{C}$ | | 7.3 | |
| Pulsed Drain Current ^a | | | I_{DM} | 28 | |
| Linear Derating Factor | | | | 1.89 | W/ $^{\circ}\text{C}$ |
| Single Pulse Avalanche Energy ^b | | | E_{AS} | 86 | mJ |
| Maximum Power Dissipation | | | P_D | 109 | W |
| Operating Junction and Storage Temperature Range | | | T_J, T_{stg} | -55 to +150 | $^{\circ}\text{C}$ |
| Drain-Source Voltage Slope | $T_J = 125\text{ }^{\circ}\text{C}$ | | dV/dt | 50 | V/ns |
| Reverse Diode dV/dt ^d | | | | 3.2 | |
| Soldering Recommendations (Peak Temperature) ^c | for 10 s | | | 300 | $^{\circ}\text{C}$ |


Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ °C}$, $L = 28.2\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 3.5\text{ A}$.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, $dI/dt = 100\text{ A}/\mu\text{s}$, starting $T_J = 25\text{ °C}$.

THERMAL RESISTANCE RATINGS

| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
|----------------------------------|------------|------|------|------|
| Maximum Junction-to-Ambient | R_{thJA} | - | 72 | °C/W |
| Maximum Junction-to-Case (Drain) | R_{thJC} | - | 0.7 | |

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|----------------------------------|---|---|------|------|-------|------|
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | V _{DS} | V _{GS} = 0 V, I _D = 250 μA | | 900 | - | - | V |
| V _{DS} Temperature Coefficient | ΔV _{DS} /T _J | Reference to 25 °C, I _D = 1 mA | | - | 0.65 | - | V/°C |
| Gate-Source Threshold Voltage (N) | V _{GS(th)} | V _{DS} = V _{GS} , I _D = 250 μA | | 2 | - | 4 | V |
| Gate-Source Leakage | I _{GSS} | V _{GS} = ± 20 V | | - | - | ± 100 | nA |
| | | V _{GS} = ± 30 V | | - | - | ± 1 | μA |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} = 900 V, V _{GS} = 0 V | | - | - | 1 | μA |
| | | V _{DS} =620 V, V _{GS} = 0 V, T _J = 125 °C | | - | - | 10 | |
| Drain-Source On-State Resistance | R _{DS(on)} | V _{GS} = 10 V | I _D = 6 A | - | 0.75 | - | Ω |
| Forward Transconductance | g _{fs} | V _{DS} = 30 V, I _D = 6 A | | - | 19 | - | S |
| Dynamic | | | | | | | |
| Input Capacitance | C _{iss} | V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz | | - | 373 | - | pF |
| Output Capacitance | C _{oss} | | | - | 26 | - | |
| Reverse Transfer Capacitance | C _{rss} | | | - | 14 | - | |
| Effective Output Capacitance, Energy Related ^a | C _{o(er)} | V _{DS} = 0 V to 520 V, V _{GS} = 0 V | | - | 46 | - | pF |
| Effective Output Capacitance, Time Related ^b | C _{o(tr)} | | | - | 64 | - | |
| Total Gate Charge | Q _g | V _{GS} = 10 V | I _D = 6 A, V _{DS} = 520 V | - | 26 | - | nC |
| Gate-Source Charge | Q _{gs} | | | - | 2.1 | - | |
| Gate-Drain Charge | Q _{gd} | | | - | 2.8 | - | |
| Turn-On Delay Time | t _{d(on)} | V _{DD} = 620 V, I _D = 6 A, V _{GS} = 10 V, R _g = 9.1 Ω | | - | 26 | - | ns |
| Rise Time | t _r | | | - | 55.7 | - | |
| Turn-Off Delay Time | t _{d(off)} | | | - | 71 | - | |
| Fall Time | t _f | | | - | 41 | - | |
| Gate Input Resistance | R _g | f = 1 MHz, open drain | | - | 3.5 | - | Ω |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous Source-Drain Diode Current | I _S | MOSFET symbol showing the integral reverse p - n junction diode  | | - | - | 7 | A |
| Pulsed Diode Forward Current | I _{SM} | | | - | - | 18 | |
| Diode Forward Voltage | V _{SD} | T _J = 25 °C, I _S = 6 A, V _{GS} = 0 V | | - | - | 1.4 | V |
| Reverse Recovery Time | t _{rr} | T _J = 25 °C, I _F = I _S = 6 A, dI/dt = 100 A/μs, V _R = 400 V | | - | 192 | - | ns |
| Reverse Recovery Charge | Q _{rr} | | | - | 2.4 | - | μC |
| Reverse Recovery Current | I _{RRM} | | | - | 11 | - | A |

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
 b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

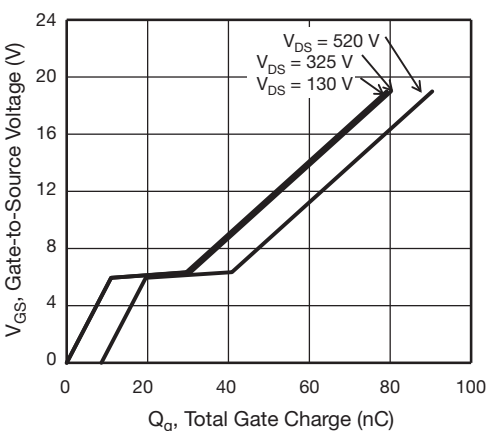
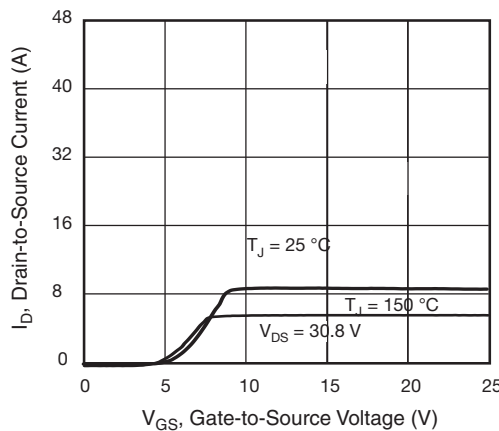
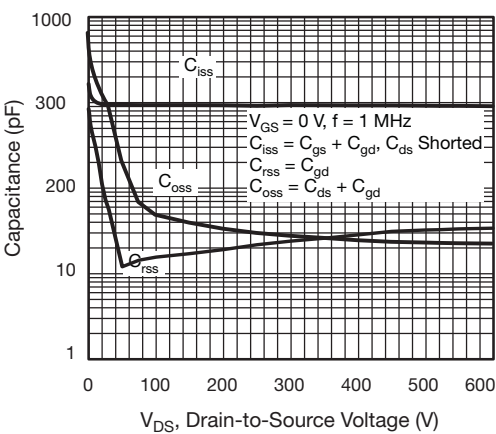
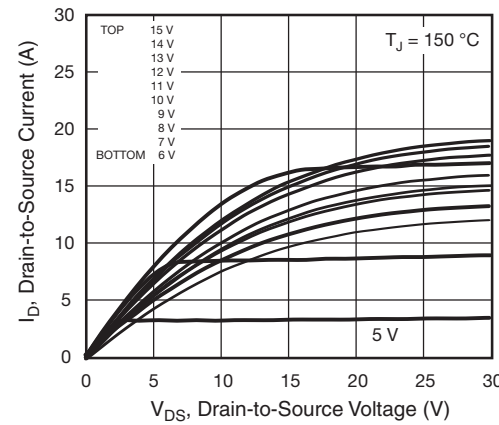
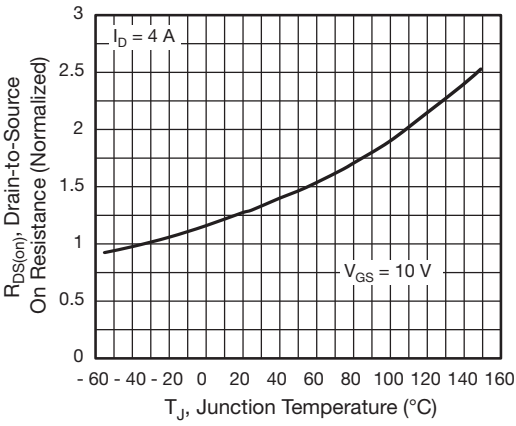
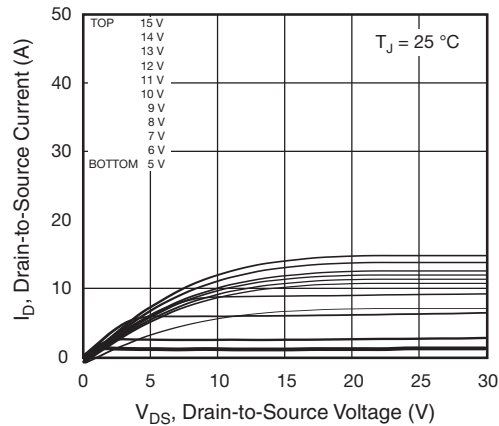




Fig. 7 - Typical Source-Drain Diode Forward Voltage



Fig. 9 - Maximum Drain Current vs. Case Temperature

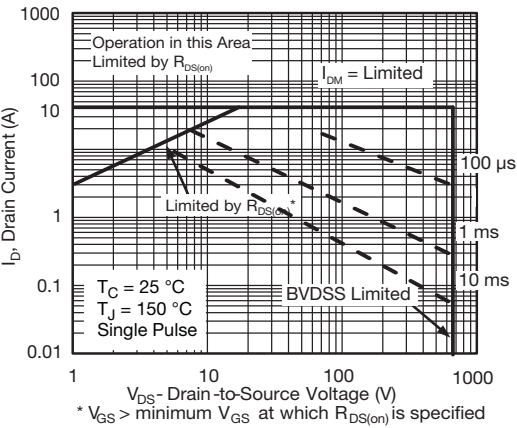


Fig. 8 - Maximum Safe Operating Area

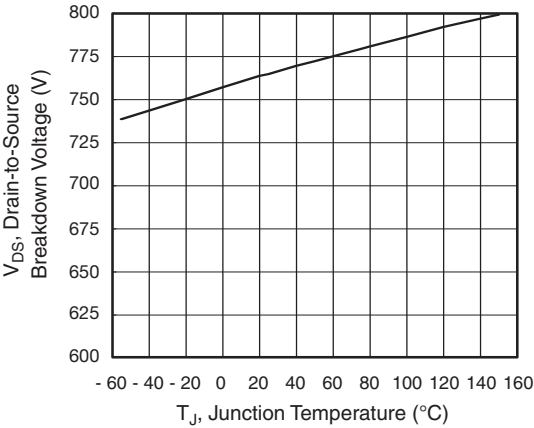


Fig. 10 - Temperature vs. Drain-to-Source Voltage



Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case



Fig. 12 - Switching Time Test Circuit



Fig. 16 - Basic Gate Charge Waveform



Fig. 13 - Switching Time Waveforms



Fig. 14 - Unclamped Inductive Test Circuit



Fig. 15 - Unclamped Inductive Waveforms

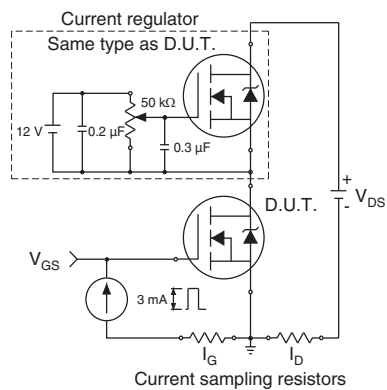


Fig. 17 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 18 - For N-Channel

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