

SUM110P04-05-VB Datasheet

P-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY

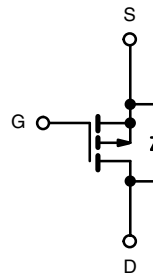
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
- 40	0.0041 at $V_{GS} = - 10$ V	- 110	185 nC

FEATURES

- Trench Power MOSFET



RoHS
COMPLIANT



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 40	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 175^\circ\text{C}$)	I_D	$T_C = 25^\circ\text{C}$ - 110 ^a	A
		$T_C = 70^\circ\text{C}$ - 110 ^a	
		$T_A = 25^\circ\text{C}$ 39 ^{b, c}	
		$T_A = 70^\circ\text{C}$ 33 ^{b, c}	
Pulsed Drain Current	I_{DM}	240	mJ
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$ 110	
		$T_A = 25^\circ\text{C}$ 10 ^{b, c}	
Avalanche Current	I_{AS}	75	
Single-Pulse Avalanche Energy	E_{AS}	281	
Maximum Power Dissipation	P_D	$T_C = 25^\circ\text{C}$ 375	W
		$T_C = 70^\circ\text{C}$ 262	
		$T_A = 25^\circ\text{C}$ 15 ^{b, c}	
		$T_A = 70^\circ\text{C}$ 10.5 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 175	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	R_{thJA}	8	10	$^\circ\text{C/W}$
Maximum Junction-to-Case (Drain)	R_{thJC}	0.33	0.4	

Notes:

a. Package limited.

b. Surface Mounted on 1" x 1" FR4 board.

c. $t = 10$ s.

d. Maximum under Steady State conditions is 40°C/W .

SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 40			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 40		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 5.5		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 2	- 3	- 4	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 40 V, V _{GS} = 0 V			- 1	μA
		V _{DS} = - 40 V, V _{GS} = 0 V, T _J = 55 °C			- 10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = - 10 V	- 120			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = - 10 V, I _D = - 20 A		0.0041		Ω
Forward Transconductance ^a	g _{fs}	V _{DS} = - 15 V, I _D = - 20 A		75		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = - 25 V, V _{GS} = 0 V, f = 1 MHz		11300		pF
Output Capacitance	C _{oss}			1510		
Reverse Transfer Capacitance	C _{rss}			1000		
Total Gate Charge	Q _g	V _{DS} = - 20 V, V _{GS} = - 10 V, I _D = - 110 A		185	280	nC
Gate-Source Charge	Q _{gs}			48		
Gate-Drain Charge	Q _{gd}			42		
Gate Resistance	R _g	f = 1 MHz		4.0		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 20 V, R _L = 0.18 Ω I _D ≅ - 110 A, V _{GEN} = - 10 V, R _g = 1 Ω		25	40	ns
Rise Time	t _r			290	440	
Turn-Off Delay Time	t _{d(off)}			110	165	
Fall Time	t _f			35	55	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			- 110	A
Pulse Diode Forward Current ^a	I _{SM}				- 240	
Body Diode Voltage	V _{SD}	I _S = - 20 A		- 0.8	- 1.5	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = - 20 A, di/dt = 100 A/μs, T _J = 25 °C		70	105	ns
Body Diode Reverse Recovery Charge	Q _{rr}			130	200	nC
Reverse Recovery Fall Time	t _a			37		ns
Reverse Recovery Rise Time	t _b			33		

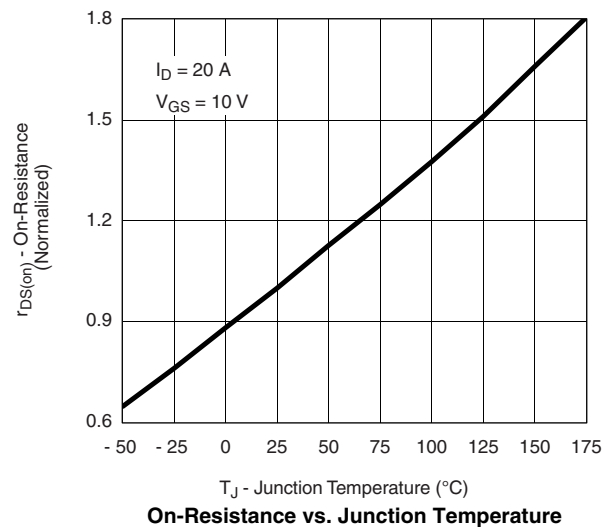
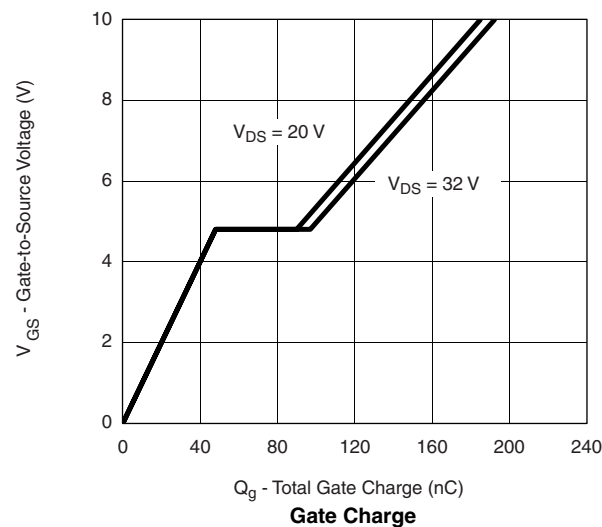
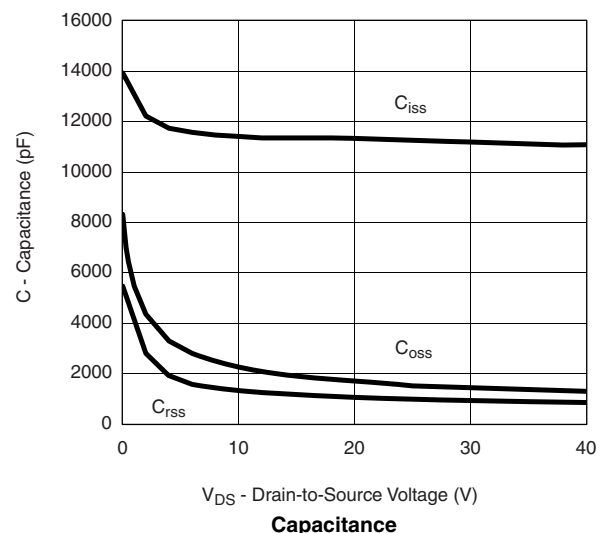
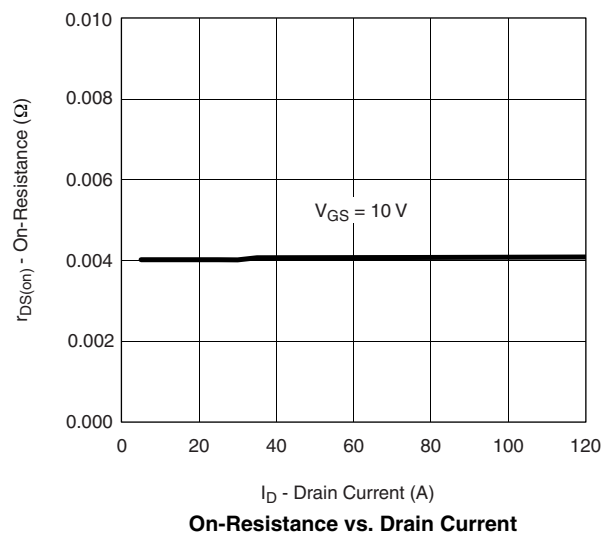
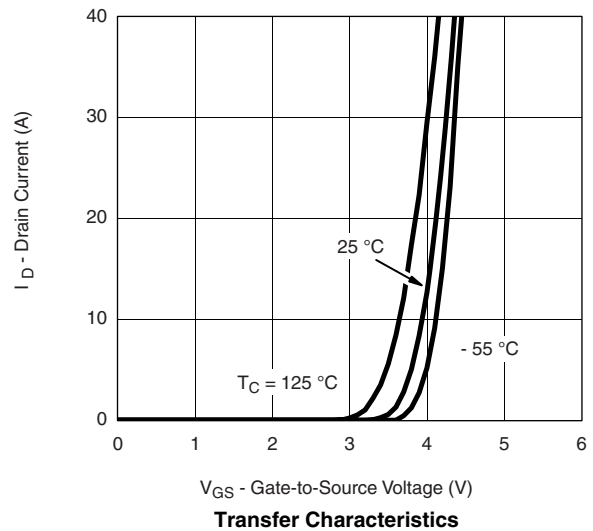
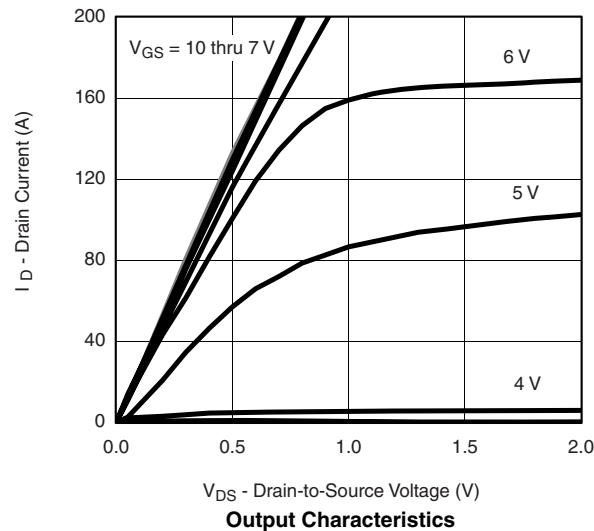
Notes:

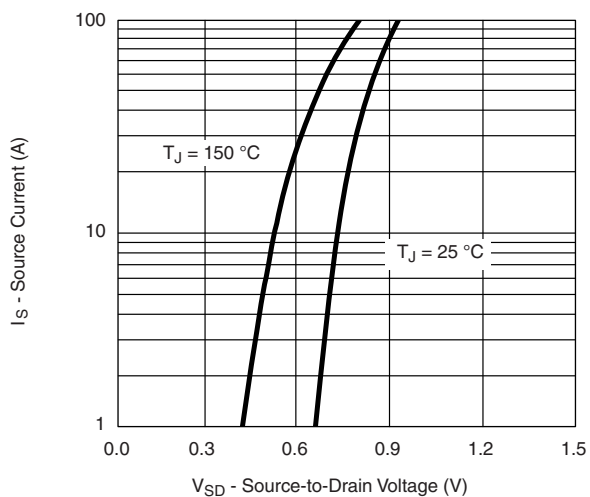
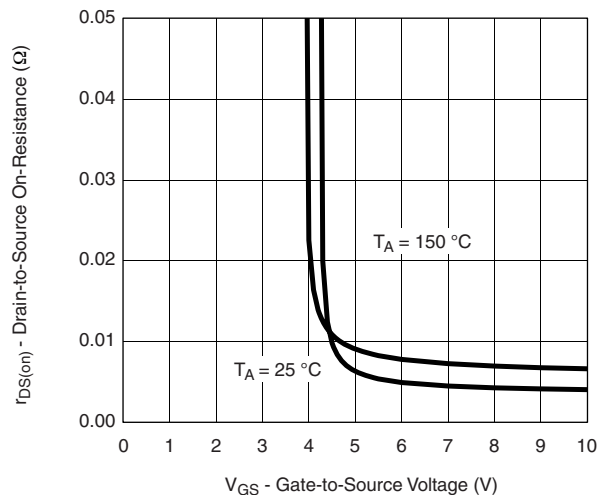
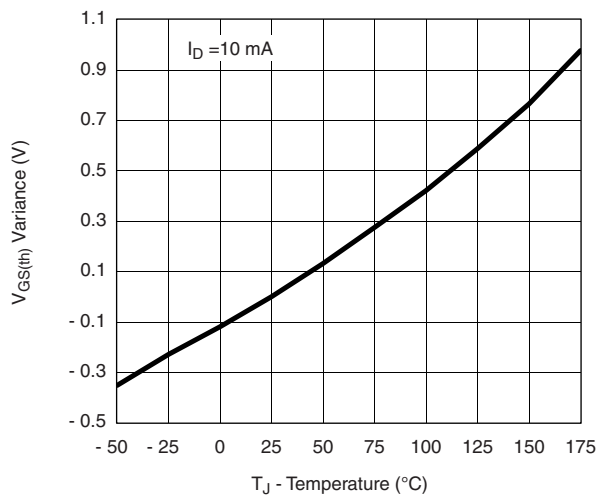
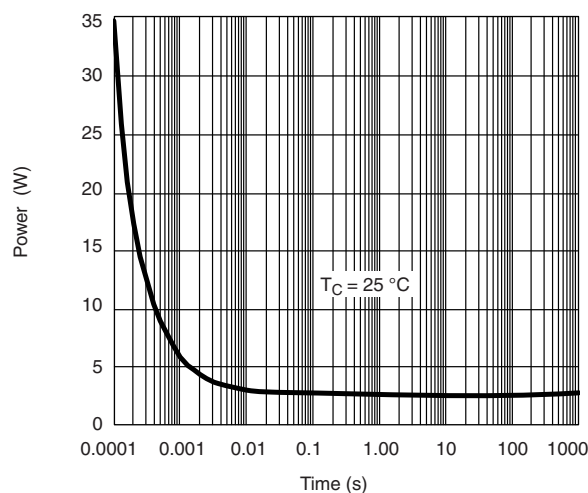
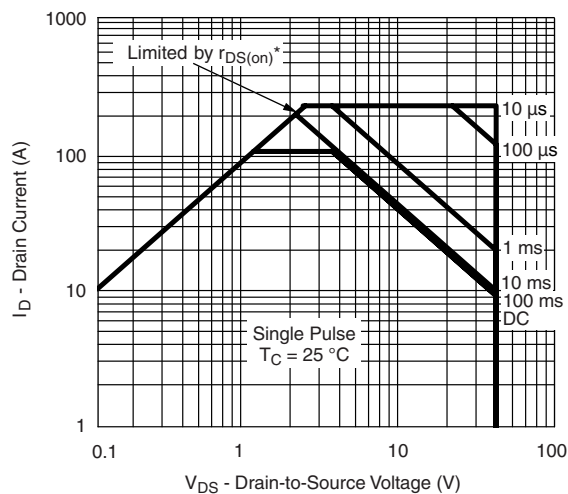
a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

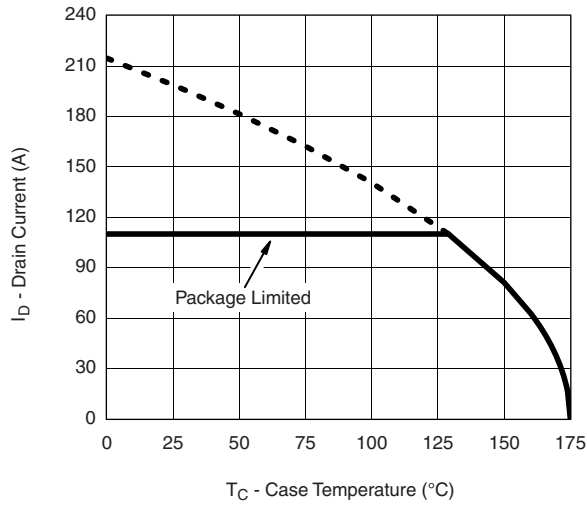


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Single Pulse Power, Junction-to-Ambient


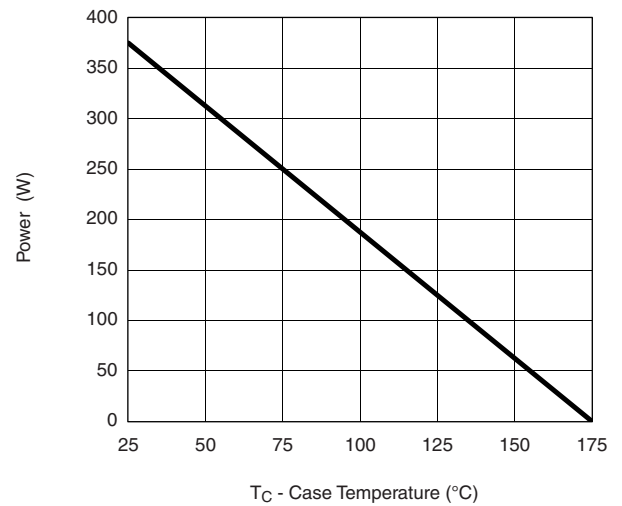
* $V_{GS} >$ minimum V_{GS} at which $r_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Case

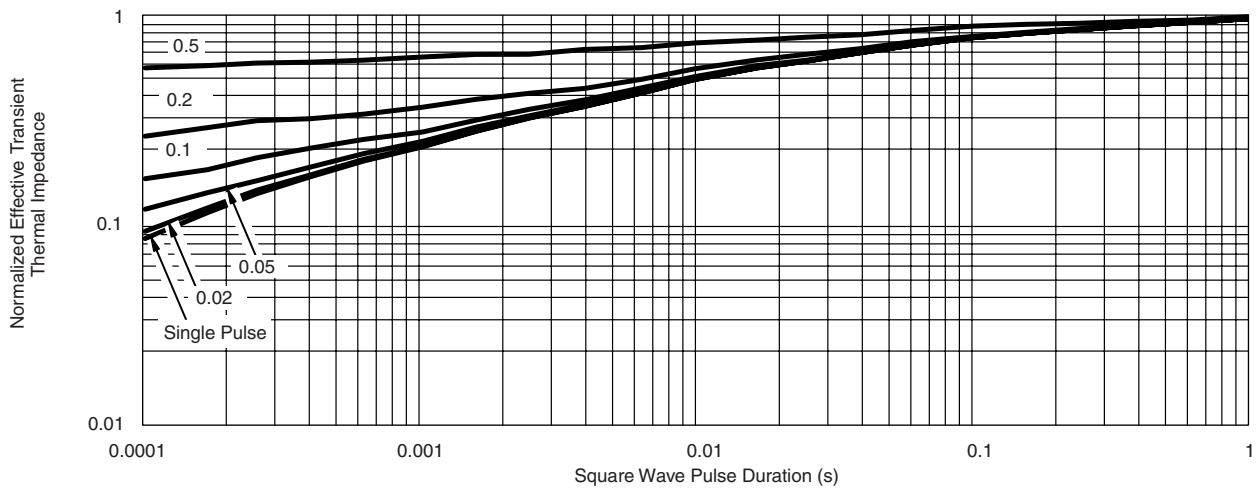
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Max. Avalanche and Drain Current vs. Case Temperature*

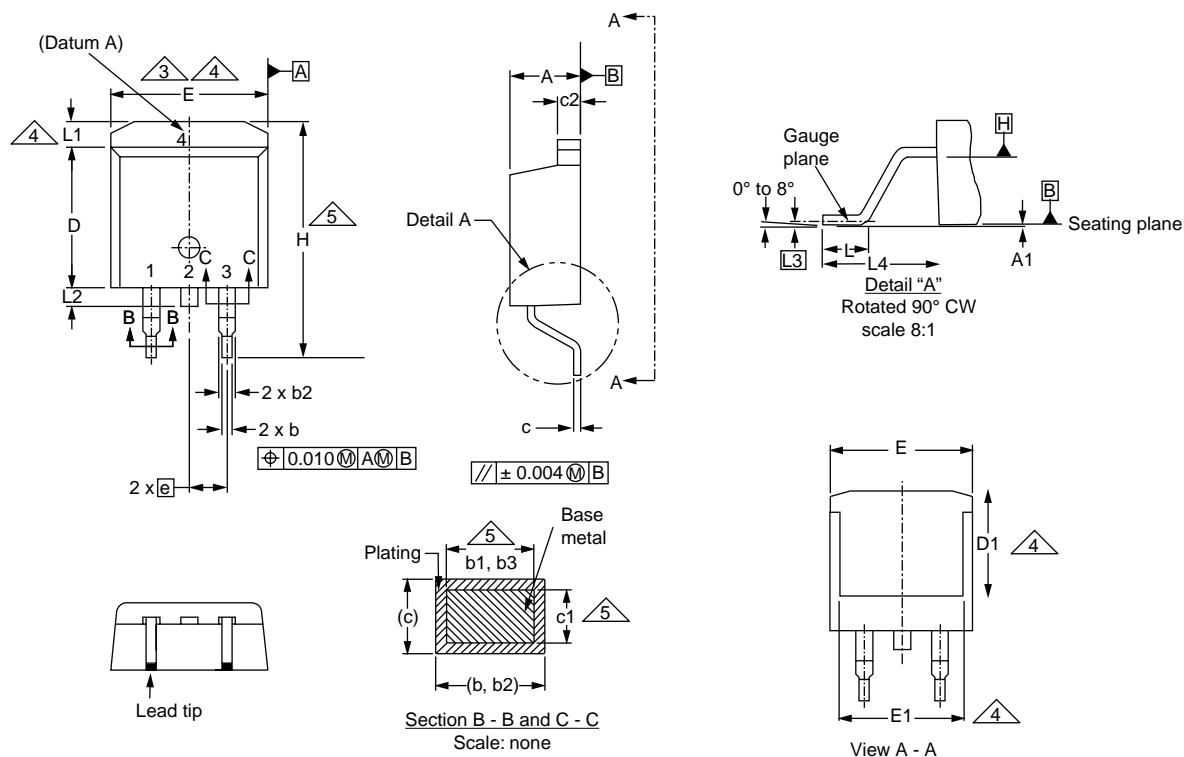


Power Derating, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Case

* The power dissipation P_D is based on $T_{J(max)} = 175$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TO-263AB

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
 DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

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