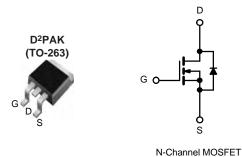


STB130NH02LT4-VB Datasheet N-Channel 30-V (D-S) MOSFET

PRODU	CT SUMMARY		
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^{a, e}	Q _g (Typ)
30	0.0024 at V _{GS} = 10 V	98	82 nC
30	0.0027 at V _{GS} = 4.5 V	98	02 110



FEATURES

- Trench Power MOSFET .
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2011/65/EU

APPLICATIONS

- OR-ing
- Server
- DC/DC •

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	30			
Gate-Source Voltage	V _{GS}	± 20	V		
	T _C = 25 °C		98 ^{a, e}		
Continuous Drain Current (T ₁ = 175 °C)	T _C = 70 °C		98 ^e		
Continuous Drain Current $(1_j = 175 \text{ C})$	T _A = 25 °C	I _D	28.8 ^{b, c}	Α	
	T _A = 70 °C		27 ^{b, c}		
Pulsed Drain Current	I _{DM}	300			
Avalanche Current Pulse		I _{AS}	36		
Single Pulse Avalanche Energy	L = 0.1 mH	E _{AS}	64.8	V	
Continuous Source-Drain Diode Current	T _C = 25 °C	I _S	90 ^{a, e}	A	
Continuous Source-Drain Diode Current	T _A = 25 °C	'S	3.13 ^{b, c}	— A	
	T _C = 25 °C		250 ^a		
Movimum Dower Dissinction	T _C = 70 °C	P _D	175	14/	
Maximum Power Dissipation	T _A = 25 °C	٢D	3.75 ^{b, c}	W	
	T _A = 70 °C		2.63 ^{b, c}		
Operating Junction and Storage Temperature R	T _J , T _{stg}	- 55 to 175	°C		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Тур.	Max.	Unit	
Maximum Junction-to-Ambient ^{b, d}	$t \le 10 \text{ sec}$	R _{thJA}	32	40	°C/W	
Maximum Junction-to-Case	Steady State	R _{thJC}	0.5	0.6	C/W	

Notes:

a. Based on $T_C = 25 \text{ °C}$. b. Surface mounted on 1" x 1" FR4 board.

c. t = 10 sec.
d. Maximum under steady state conditions is 90 °C/W.
e. Calculated based on maximum junction temperature. Package limitation current is 90 A.



SPECIFICATIONS ($T_J = 25 \ ^{\circ}C$,			1			-
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static	-		1			
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$	30			V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250 μA		35		mV/°C
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	-		- 7.5		
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	1.5		2.5	V
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V$, $V_{GS} = \pm 20 V$			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			1	μA
Zero Gale Voltage Drain Gurrent	1055	V_{DS} = 30 V, V_{GS} = 0 V, T_{J} = 55 °C			10	μΛ
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, \text{ V}_{GS} = 10 \text{ V}$	90			А
Drain Course On State Desister and	Real	V _{GS} = 10 V, I _D = 28.8 A		0.0024		0
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 27 \text{ A}$		0.0027		Ω
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 28.8 A		160		S
Dynamic ^b						
Input Capacitance	C _{iss}			12065		
Output Capacitance	C _{oss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz		1725		pF
Reverse Transfer Capacitance	C _{rss}			970		
Tatal Cata Channa		V_{DS} = 15 V, V_{GS} = 10 V, I_{D} = 28.8 A		171	257	nC
Total Gate Charge	Qg			81.5	123	
Gate-Source Charge	Q _{gs}	V_{DS} = 15 V, V_{GS} = 4.5 V, I_{D} = 28.8 A		34		
Gate-Drain Charge	Q _{gd}			29		
Gate Resistance	R _g	f = 1 MHz		1.4	2.1	Ω
Turn-On Delay Time	t _{d(on)}			18	27	
Rise Time	t _r	V_{DD} = 15 V, R_L = 0.625 Ω		11	17	
Turn-Off Delay Time	t _{d(off)}	$\text{I}_{\text{D}}\cong$ 24 A, V_{GEN} = 10 V, R_{g} = 1 Ω		70	105	
Fall Time	t _f			10	15	
Turn-On Delay Time	t _{d(on)}			55	83	ns
Rise Time	t _r	V_{DD} = 15 V, R _L = 0.67 Ω		180	270	_
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 22.5 \text{ A}, \text{ V}_{\text{GEN}} = 4.5 \text{ V}, \text{ R}_{\text{g}} = 1 \Omega$		55	83	1
Fall Time	t _f			12	18	
Drain-Source Body Diode Characteristic	s		1			
Continuous Source-Drain Diode Current	۱ _S	T _C = 25 °C			90	
Pulse Diode Forward Current ^a	I _{SM}				90	A
Body Diode Voltage	V _{SD}	I _S = 22 A		0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}			52	78	ns
Body Diode Reverse Recovery Charge	Q _{rr}			70.2	105	nC
Reverse Recovery Fall Time	t _a	$I_F = 20 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 \text{ °C}$		27		- ns
Reverse Recovery Rise Time	t _b			25		

Notes:

a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.

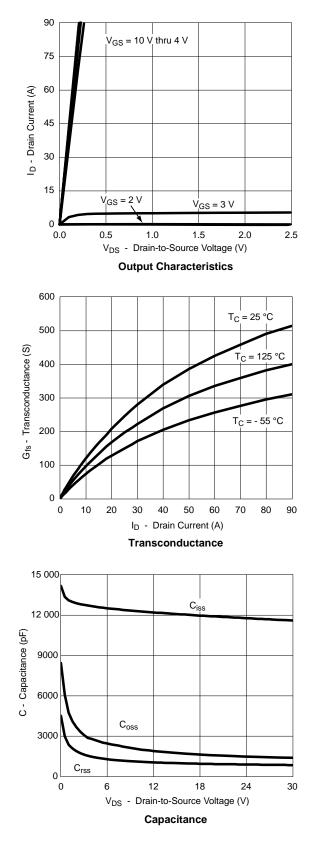
b. Guaranteed by design, not subject to production testing.

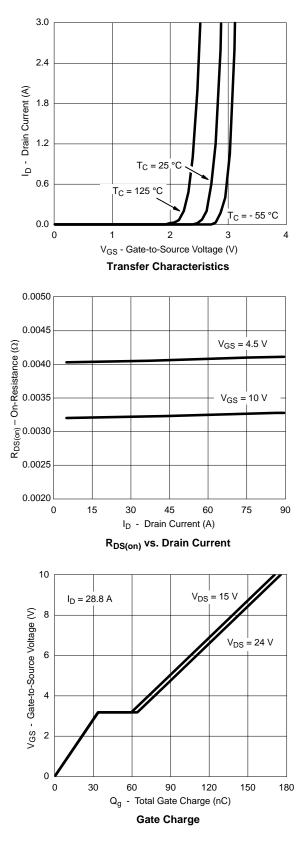
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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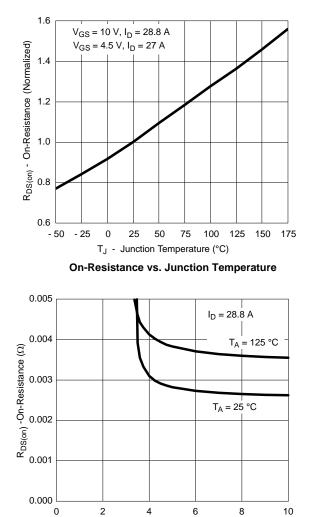




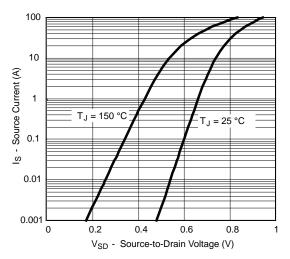




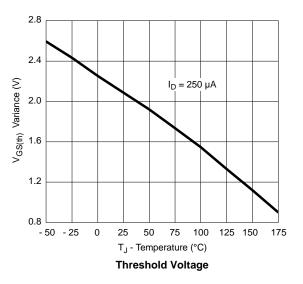
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

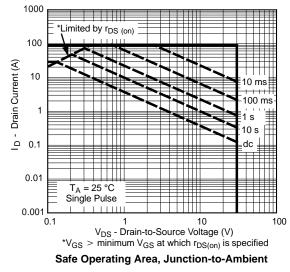


 V_{GS} - Gate-to-Source Voltage (V) R_{DS(on)} vs. V_{GS} vs. Temperature

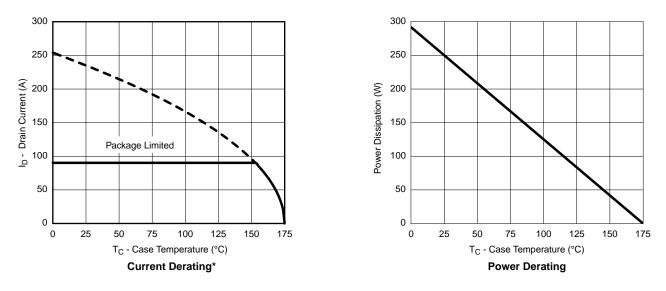


Forward Diode Voltage vs. Temperature



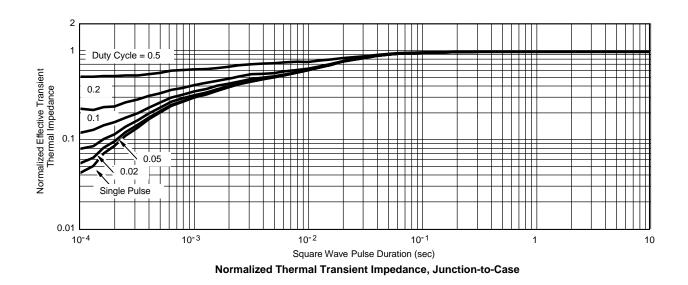






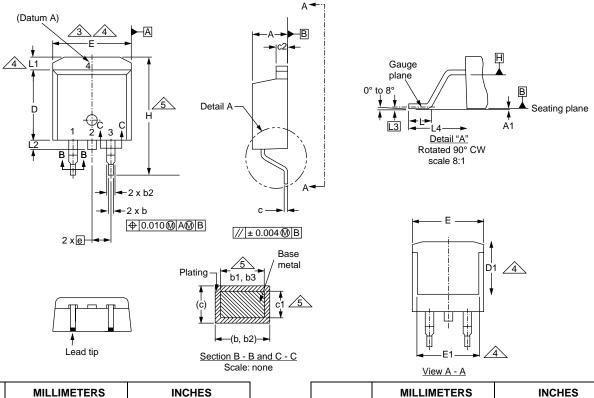
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

*The power dissipation P_D is based on $T_{J(max)} = 175$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





TO-263AB (HIGH VOLTAGE)



	MILLIMETERS		INCHES			MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.	DIM.	MIN.	MAX.	MIN.	MAX
А	4.06	4.83	0.160	0.190	D1	6.86	-	0.270	-
A1	0.00	0.25	0.000	0.010	E	9.65	10.67	0.380	0.42
b	0.51	0.99	0.020	0.039	E1	6.22	-	0.245	-
b1	0.51	0.89	0.020 0.035		е	2.54 BSC		0.100) BSC
b2	1.14	1.78	0.045	0.070	Н	14.61	15.88	0.575	0.62
b3	1.14	1.73	0.045	0.068	L	1.78	2.79	0.070	0.11
С	0.38	0.74	0.015	0.029	L1	-	1.65	-	0.06
c1	0.38	0.58	0.015	0.023	L2	-	1.78	-	0.07
c2	1.14	1.65	0.045	0.065	L3	0.25 BSC		0.010 BSC	
D	8.38	9.65	0.330	0.380	L4	4.78	5.28	0.188	0.20

Notes

2. Dimensions are shown in millimeters (inches).

3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.

4. Thermal PAD contour optional within dimension E, L1, D1 and E1.

5. Dimension b1 and c1 apply to base metal only.

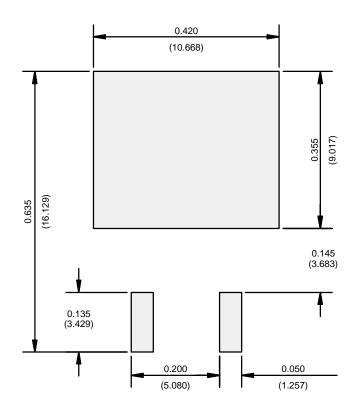
6. Datum A and B to be determined at datum plane H.

7. Outline conforms to JEDEC outline to TO-263AB.

^{1.} Dimensioning and tolerancing per ASME Y14.5M-1994.



RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)



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