

SPB80N04S2L-03-VB Datasheet

N-Channel 40 V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	$R_{DS(on)}$ (Ω)	I _D (A) ^{a, c}	Q _g (Typ.)	
40	0.0017 at V _{GS} = 10 V	150	120 nC	
	0.0025 at V _{GS} = 4.5 V	135	120110	

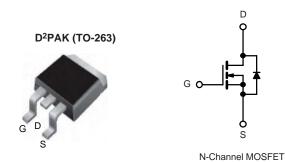
FEATURES

- Trench Power MOSFET
- 100 % R_g and UIS Tested



APPLICATIONS

- Synchronous Rectification
- Power Supplies



ABSOLUTE MAXIMUM RATING	S T _A = 25 °C, unle	ss otherwise note	ed	
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	40	V	
Gate-Source Voltage	V _{GS}	± 25		
	T _C = 25 °C		150 ^{a, c}	
Continuous Prain Current (T. – 175 °C)	T _C = 70 °C		120 ^c	
Continuous Drain Current (T _J = 175 °C)	T _A = 25 °C	I _D	29 ^b	A
	T _A = 70 °C		23 ^b	A
Pulsed Drain Current		I _{DM}	380	
Avalanche Current Pulse	1 0.1 ml l	I _{AS}	80	
Single Pulse Avalanche Energy L = 0.1 mH		E _{AS}	320	mJ
0 " 0 D D D D D D	T _C = 25 °C		110 ^{a, c}	^
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	2.6 ^b	A
	T _C = 25 °C		312 ^a	
Maximum Power Dissipation	T _C = 70 °C		200	10/
	T _A = 25 °C	P _D	3.13 ^b	W
	T _A = 70 °C		2.0 ^b	
Operating Junction and Storage Temperature R	T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^b	Steady State	R _{thJA}	32	40	°C/W	
Maximum Junction-to-Case	Steady State	R_{thJC}	0.33	0.4	C/VV	

Notes:

- a. Based on $T_C = 25$ °C.
- b. Surface Mounted on 1" x 1" FR4 board.
- c. Calculated based on maximum junction temperature. Package limitation current is 110 $\,\mathrm{A.}$

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1



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static	•					
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	45			V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250 μA		41		mV/°C
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 8		
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.2		2.5	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$			1	
		$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			10	μA
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	120			Α
Drain-Source On-State Resistance ^a	D	V _{GS} = 10 V, I _D = 30 A		0.0017		Ω
	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$		0.0025		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 30 A		180		S
Dynamic ^b				•		
Input Capacitance	C _{iss}			9000		pF
Output Capacitance	C _{oss}	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		650		
Reverse Transfer Capacitance	C _{rss}			450		
Total Gate Charge	Q_{g}			120	180	nC
Gate-Source Charge	Q _{gs}	$V_{DS} = 20 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 20 \text{ A}$		30		
Gate-Drain Charge	Q _{gd}			16		
Gate Resistance	R_{g}	f = 1 MHz		0.85	1.3	Ω
Turn-On Delay Time	t _{d(on)}			20	30	
Rise Time	t _r	V_{DD} = 20 V, R_L = 1.0 Ω		11	17	ns
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 20 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		77	115	
Fall Time	t _f			10	15	
Turn-On Delay Time	t _{d(on)}			102	155	
Rise Time	t _r	V_{DD} = 20 V, R_L = 1.0 Ω		62	95	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 20 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		180	270	
Fall Time	t _f			60	90	
Drain-Source Body Diode Characteristic	s					
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			110	^
Pulse Diode Forward Current ^a	I _{SM}				200	Α
Body Diode Voltage	V _{SD}	I _S = 20 A		0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}			50	75	ns
Body Diode Reverse Recovery Charge	Q _{rr}			70	105	nC
Reverse Recovery Fall Time	t _a	$I_F = 20 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		30		ns
Reverse Recovery Rise Time	t _b	1		20		

Notes:

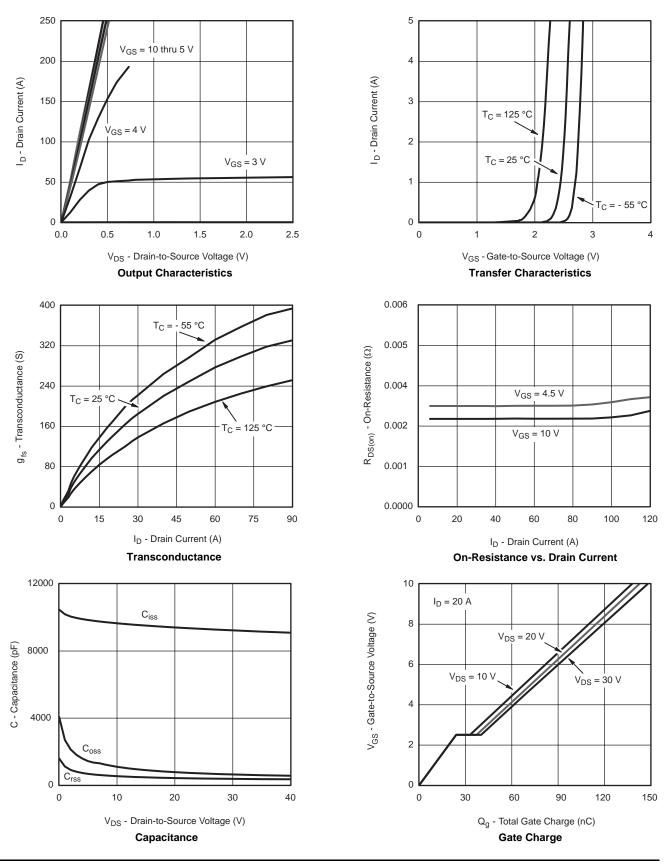
- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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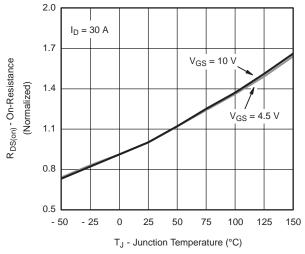


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

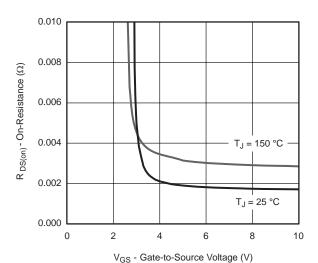




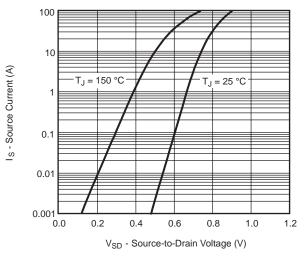
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



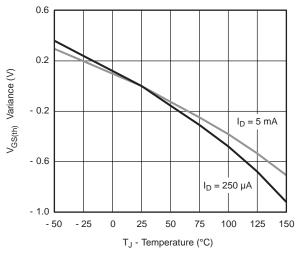
On-Resistance vs. Junction Temperature



On-Resistance vs. Gate-to-Source Voltage



Forward Diode Voltage vs. Temperature



Threshold Voltage

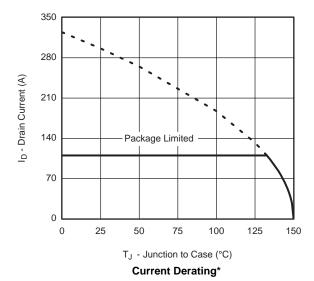


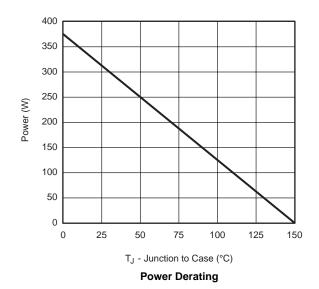
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

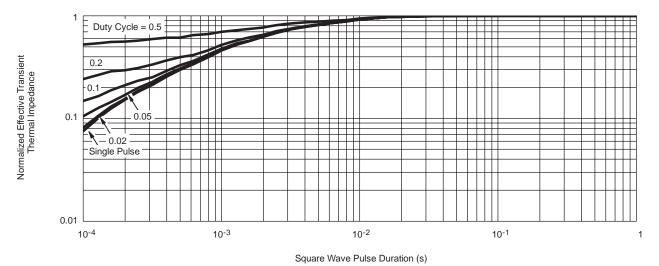


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





^{*} The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

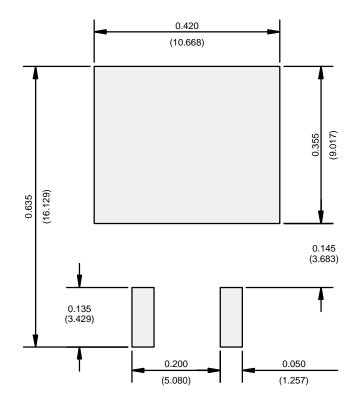


Normalized Thermal Transient Impedance, Junction-to-Case

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RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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