

PSMN1R7-60BS-VB Datasheet N-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	60			
$R_{DS(on)} (\Omega)$ at $V_{GS} = 10 V$	0.0025			
$R_{DS(on)} (\Omega)$ at $V_{GS} = 4.5 V$	0.0070			
I _D (A)	270			
Configuration	Single			

FEATURES

- TrenchFET[®] power MOSFET
- Package with low thermal resistance
- 100 % $\rm R_g$ and UIS tested





ABSOLUTE MAXIMUM RATING				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V _{DS}	60	V
Gate-Source Voltage		V _{GS}	± 20	
Continuous Drain Current	T _C = 25 °C	- I _D	270	A
	T _C = 125 °C		120 ^a	
Continuous Source Current (Diode Conduc	tion)	I _S	120 ^a	
Pulsed Drain Current ^b		I _{DM}	600	
Single Pulse Avalanche Current		I _{AS}	75	
Single Pulse Avalanche Energy	L = 0.1 mH	E _{AS}	281	mJ
	T _C = 25 °C	D	375	w
Maximum Power Dissipation ^b	T _C = 125 °C	P _D	125	vv
Operating Junction and Storage Temperatu	ure Range	T _J , T _{sta}	-55 to +175	°C

THERMAL RESISTANCE RATINGS							
PARAMETER		SYMBOL	LIMIT	UNIT			
Junction-to-Ambient	PCB Mount ^c	R _{thJA}	40	°C/W			
Junction-to-Case (Drain)			0.4	0/10			

Notes

a. Package limited.

b. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

c. When mounted on 1" square PCB (FR4 material).



SPECIFICATIONS ($T_C = 25 \ ^{\circ}C$,	unless otherv	vise noted)		0	T			
PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT		
Static								
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$		60	-	-	v	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS}=V_{GS},I_{D}=250\;\mu A$		1.5	2.0	2.5		
Gate-Source Leakage	I _{GSS}	$V_{DS}=0~V,~V_{GS}=\pm~20~V$		-	-	± 100	nA	
		$V_{GS} = 0 V$	$V_{DS} = 60 V$	-	-	1	μA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{GS} = 0 V$	$V_{DS}=60~V,~T_J=125~^\circ C$	-	-	50	μΑ	
		$V_{GS} = 0 V$	V_{DS} = 60 V, T_J = 175 °C	-	-	1.5	mA	
On-State Drain Current ^a	I _{D(on)}	$V_{GS} = 10 V$	$V_{DS} \ge 5 V$	120	-	-	А	
		$V_{GS} = 10 \text{ V}$	I _D = 30 A	-	0.0025	I		
Drain-Source On-State Resistance ^a	P	$V_{GS} = 10 V$	$I_D = 30 \text{ A}, \text{T}_\text{J} = 125 \ ^\circ\text{C}$	-	0.0040	-	Ω	
Drain-Source On-State Resistance "	R _{DS(on)}	$V_{GS} = 10 V$	$I_D = 30 \text{ A}, T_J = 175 \ ^\circ\text{C}$	-	0.0075	-		
		$V_{GS} = 4.5 V$	I _D = 20 A	-	0.0070	-		
Forward Transconductance b	9 _{fs}	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 30 \text{ A}$		-	164	-	S	
Dynamic ^b		·						
Input Capacitance	C _{iss}		V _{DS} = 25 V, f = 1 MHz	-	9000	-	pF	
Output Capacitance	C _{oss}	$V_{GS} = 0 V$		-	5750	7200		
Reverse Transfer Capacitance	C _{rss}]		-	860	1100		
Total Gate Charge ^c	Qg		$V_{GS} = 10 \text{ V}$ $V_{DS} = 30 \text{ V}, \text{ I}_{D} = 80 \text{ A}$		128	200		
Gate-Source Charge ^c	Q _{gs}	V _{GS} = 10 V			33	-	nC	
Gate-Drain Charge ^c	Q _{gd}]			11	-		
Gate Resistance	Rg	f = 1 MHz		0.8	1.68	2.6	Ω	
Turn-On Delay Time ^c	t _{d(on)}	V_{DD} = 30 V, R _L = 0.375 Ω I _D ≅ 80 A, V _{GEN} = 10 V, R _g = 1 Ω		-	20	25	ns	
Rise Time ^c	t _r			-	15	40		
Turn-Off Delay Time ^c	t _{d(off)}			-	65	100		
Fall Time ^c	t _f	1	-	12	20			
Source-Drain Diode Ratings and Chara	acteristics ^b							
Pulsed Current ^a	I _{SM}			-	-	200	Α	
Forward Voltage	V _{SD}	I _F = 80 A, V _{GS} = 0 V		-	0.88	1.5	V	

Notes

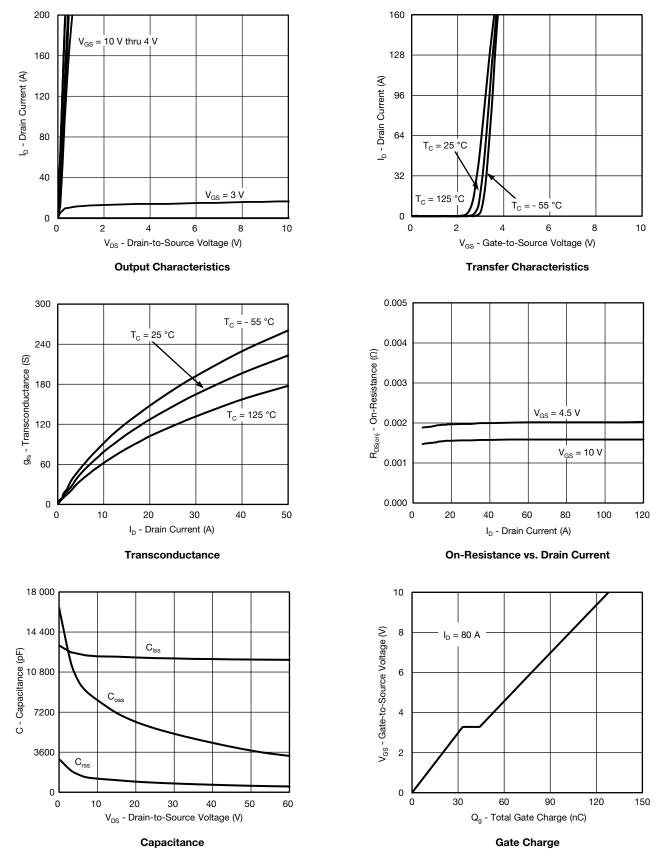
a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

c. Independent of operating temperature.

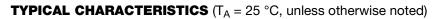


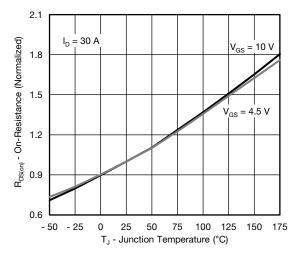
TYPICAL CHARACTERISTICS ($T_A = 25 \text{ °C}$, unless otherwise noted)



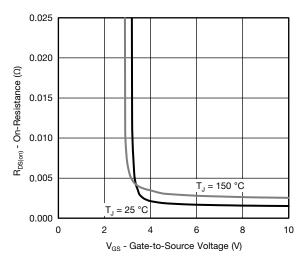
服务热线:400-655-8788



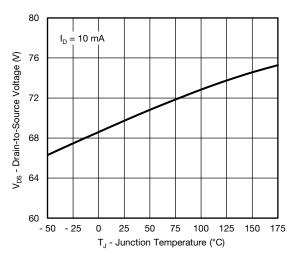




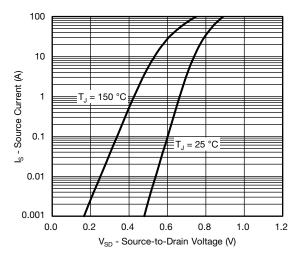
On-Resistance vs. Junction Temperature



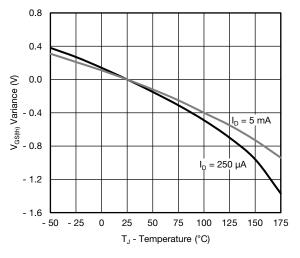
On-Resistance vs. Gate-to-Source Voltage



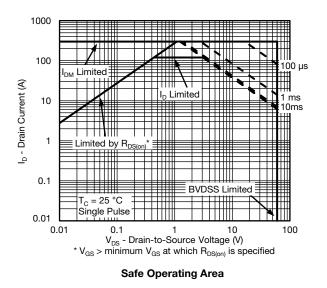
Drain Source Breakdown vs. Junction Temperature



Source Drain Diode Forward Voltage



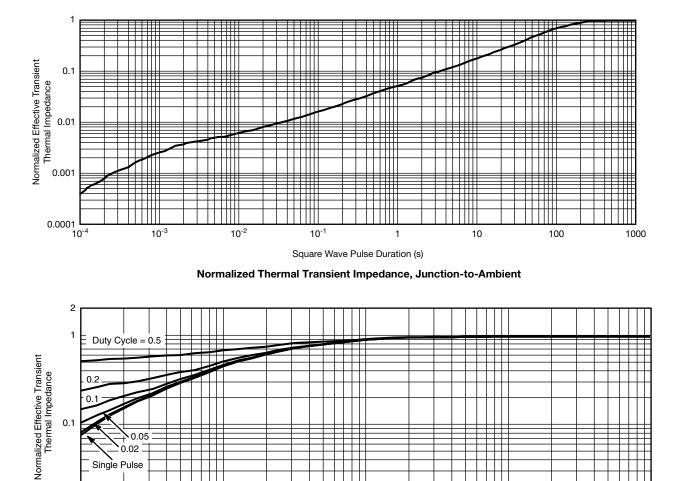


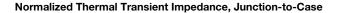


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THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)





10-1

10-2

Square Wave Pulse Duration (s)

Note

0.1

0.01 10-4

The characteristics shown in the two graphs

0.05 0.02 Single Pulse

- Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)

10⁻³

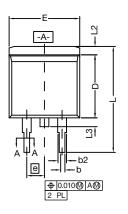
- Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

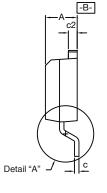
are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

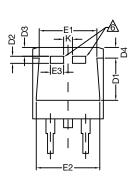
1



TO-263 (D²PAK): 3-LEAD

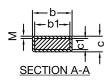








DETAIL A (ROTATED 90°)



		INC	HES	MILLIN	IETERS	
DIM.		MIN.	MAX.	MIN.	MAX.	
A		0.160	0.190	4.064	4.826	
b		0.020	0.039	0.508	0.990	
b1		0.020	0.035	0.508	0.889	
b2		0.045	0.055	1.143	1.397	
С*	Thin lead	0.013	0.018	0.330	0.457	
	Thick lead	0.023	0.028	0.584	0.711	
<u>1</u>	Thin lead	0.013	0.017	0.330	0.431	
c1	Thick lead	0.023	0.027	0.584	0.685	
c2		0.045	0.055	1.143	1.397	
	D	0.340	0.380	8.636	9.652	
D1		0.220	0.240	5.588	6.096	
D2		0.038	0.042	0.965	1.067	
D3		0.045	0.055	1.143	1.397	
D4		0.044	0.052	1.118	1.321	
E		0.380	0.410	9.652	10.414	
E1		0.245	-	6.223	-	
E2		0.355	0.375	9.017	9.525	
E3		0.072	0.078	1.829	1.981	
	е	0.100 BSC		2.54 BSC		
К		0.045	0.055	1.143	1.397	
L		0.575	0.625	14.605	15.875	
L1		0.090	0.110	2.286	2.794	
L2		0.040	0.055	1.016	1.397	
L3		0.050	0.070	1.270	1.778	
	L4	0.010 BSC		0.254 BSC		
М		-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13 DWG: 5843						

Notes

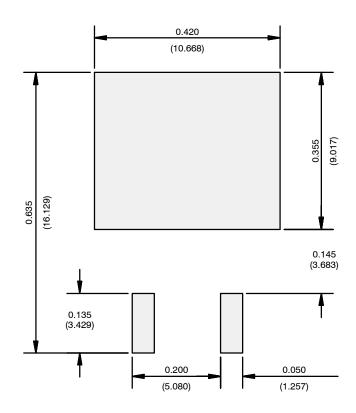
- 1. Plane B includes maximum features of heat sink tab and plastic. 2. No more than 25 % of L1 can fall above seating plane by
- max. 8 mils.3. Pin-to-pin coplanarity max. 4 mils.
- 4. *: Thin lead is for SUB, SYB.
 - Thick lead is for SUM, SYM, SQM.
- 5. Use inches as the primary measurement.

This feature is for thick lead.

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RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)



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