

# P2504ES-VB Datasheet P-Channel 40 V (D-S) MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	-40			
$R_{DS(on)}(\Omega)$ at $V_{GS} = -10 \text{ V}$	0.012			
$R_{DS(on)}(\Omega)$ at $V_{GS} = -4.5 \text{ V}$	0.015			
I <sub>D</sub> (A)	-60			
Configuration	Single			

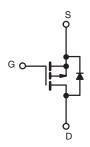
## **FEATURES**

- Trench power MOSFET
- Package with low thermal resistance
- 100 % R<sub>g</sub> and UIS tested









P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	LIMIT	UNIT			
Drain-Source Voltage		V <sub>DS</sub>	-40	V		
Gate-Source Voltage		V <sub>GS</sub>	± 20	V		
Continuous Drain Current	T <sub>C</sub> = 25 °C <sup>a</sup>	I <sub>D</sub>	-60			
Continuous Drain Current	T <sub>C</sub> = 125 °C		-45			
Continuous Source Current (Diode Conduction) a		I <sub>S</sub>	-60	Α		
Pulsed Drain Current <sup>b</sup>	I <sub>DM</sub>	-230				
Single Pulse Avalanche Current		I <sub>AS</sub>	-45			
Single Pulse Avalanche Energy L = 0.1 mH		E <sub>AS</sub>	80	mJ		
	T <sub>A</sub> = 25 °C		3.5			
Maximum Power Dissipation b	T <sub>C</sub> = 25 °C	$P_{D}$	166	W		
	T <sub>C</sub> = 125 °C		65			
Operating Junction and Storage Temperature Rar	nge	T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C		

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-Ambient	PCB Mount c	$R_{thJA}$	50	°C/W	
Junction-to-Case (Drain)		$R_{thJC}$	1.1	C/VV	

#### Notes

- a. Package limited.
- b. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.
- c. When mounted on 1" square PCB (FR4 material).
- d. Parametric verification ongoing.



PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT		
Static		•						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$		-40	-	-	.,	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-1.5	-	-2.5	V	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	0 V, V <sub>GS</sub> = ± 20 V	-	-	± 100	nA	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -40 V	-	-	-1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -40 V, T <sub>J</sub> = 125 °C	-	-	-50	μA	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -40 V, T <sub>J</sub> = 175 °C	-	-	-150		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = -10 V	V <sub>DS</sub> ≤ -5 V	-60	-	-	Α	
		V <sub>GS</sub> = -10 V	I <sub>D</sub> = -17 A	-	0.012	-	Ω	
Due in Course On Chata Basistanas		V <sub>GS</sub> = -10 V	I <sub>D</sub> = -50 A, T <sub>J</sub> = 125 °C	-	0.017	-		
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V	I <sub>D</sub> = -50 A, T <sub>J</sub> = 175 °C	-	0.020	-		
		V <sub>GS</sub> = -4.5 V	I <sub>D</sub> = -14 A	-	0.015	-		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -17 A		-	61	-	S	
Dynamic <sup>b</sup>								
Input Capacitance	C <sub>iss</sub>			-	2872	3950	pF	
Output Capacitance	Coss	$V_{GS} = 0 V$	V <sub>DS</sub> = -25 V, f = 1 MHz	-	508	635		
Reverse Transfer Capacitance	C <sub>rss</sub>			-	352	440		
Total Gate Charge <sup>c</sup>	Qg			-	60	80	nC	
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	V <sub>GS</sub> = -10 V	$V_{DS} = -30 \text{ V}, I_D = -50 \text{ A}$	-	5.7	8.6		
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			-	14.7	22		
Gate Resistance	R <sub>g</sub>	f = 1 MHz		1.5	3	4.5	Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			-	10	15		
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD}$ = -20 V, $R_L$ = 0.4 $\Omega$ $I_D$ $\cong$ -50 A, $V_{GEN}$ = -10 V, $R_g$ = 1 $\Omega$		-	12	18	ns	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	40	60		
Fall Time <sup>c</sup>	t <sub>f</sub>			-	16	24		
Source-Drain Diode Ratings and Chara	acteristics <sup>b</sup>							
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	-200	Α	
Forward Voltage	$V_{SD}$	I <sub>F</sub> =	-	-1	-1.5	V		

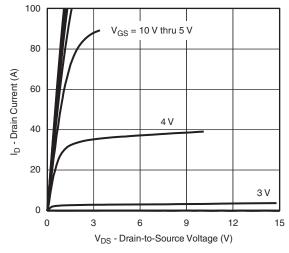
#### Notes

- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

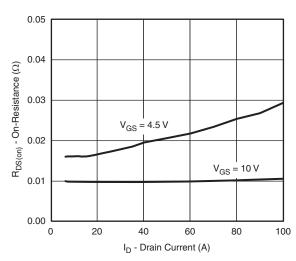
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



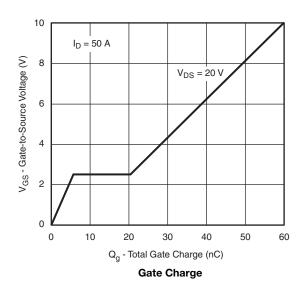
## TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)

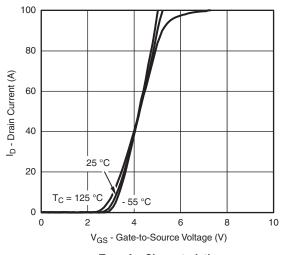


## **Output Characteristics**

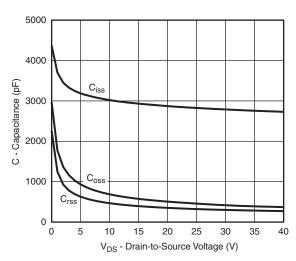


On-Resistance vs. Drain Current

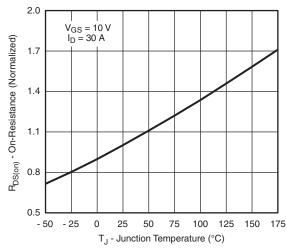




**Transfer Characteristics** 



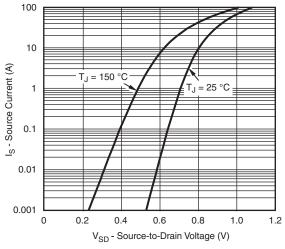
Capacitance

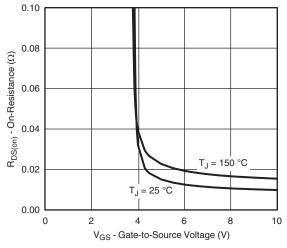


On-Resistance vs. Junction Temperature



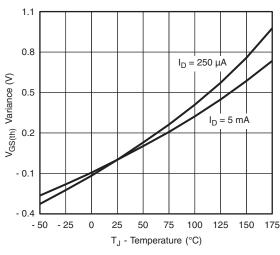
## **TYPICAL CHARACTERISTICS** ( $T_A = 25 \, ^{\circ}\text{C}$ , unless otherwise noted)

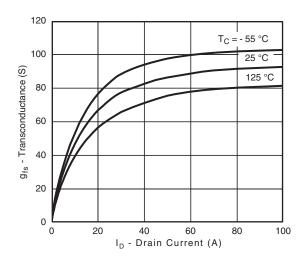




## **Source Drain Diode Forward Voltage**



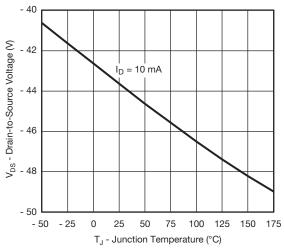




## **Threshold Voltage**

4

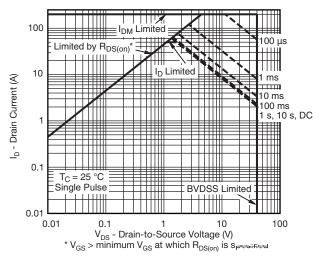
Transconductance



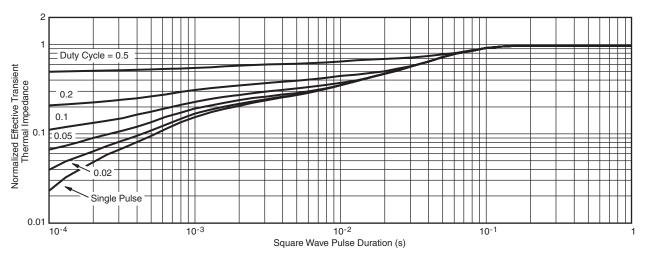
Drain Source Breakdown vs. Junction Temperature



## **TYPICAL CHARACTERISTICS** ( $T_A = 25$ °C, unless otherwise noted)



Safe Operating Area

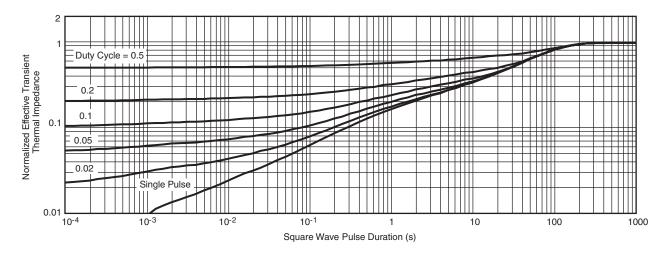


Normalized Thermal Transient Impedance, Junction-to-Case

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## Normalized Thermal Transient Impedance, Junction-to-Ambient

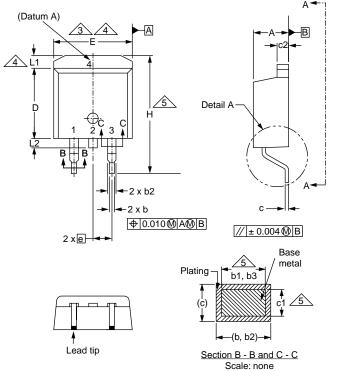
#### Note

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- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.



## **TO-263AB (HIGH VOLTAGE)**



MIN.

0.160

0.000

0.020

0.020

0.045

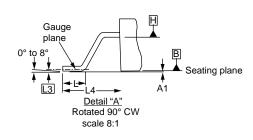
0.045

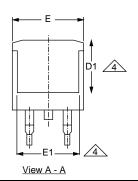
0.015

0.015

0.045

0.330





**INCHES** 

MAX.

MIN.

	2		(	)

DIM.

INC		
	MAX.	
)	0.190	
)	0.010	
)	0.039	
)	0.035	
5	0.070	
5	0.068	
5	0.029	
5	0.023	
5	0.065	
)	0.380	

D1	6.86	-	0.270	-
Е	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
е	2.54 BSC		0.100	BSC
Н	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25	BSC	0.010	BSC
L4	4.78	5.28	0.188	0.208

MAX.

**MILLIMETERS** 

MIN.

8.38 ECN: S-82110-Rev. A, 15-Sep-08

DWG: 5970

DIM.

Α Α1

b b1

b2

b3

С

c1 c2

D

#### **Notes**

1. Dimensioning and tolerancing per ASME Y14.5M-1994.

**MILLIMETERS** 

MAX.

4.83

0.25

0.99

0.89

1.78

1.73

0.74

0.58

1.65

9.65

MIN.

4.06

0.00

0.51

0.51

1.14

1.14

0.38

0.38

1.14

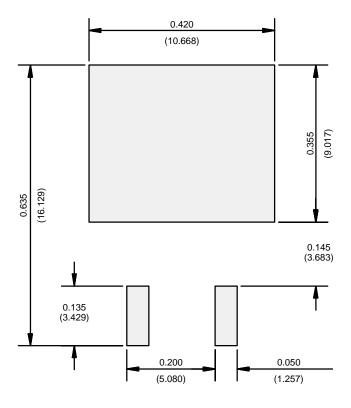
- 2. Dimensions are shown in millimeters (inches).
- 3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
- 4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
- 5. Dimension b1 and c1 apply to base metal only.
- 6. Datum A and B to be determined at datum plane H.
- 7. Outline conforms to JEDEC outline to TO-263AB.

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## RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)



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