

IRFZ34NSTR-VB Datasheet

N-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY

| V_{DS} (V) | $R_{DS(on)}$ (Ω) | I_D (A) ^{a, e} | Q_g (Max) |
|--------------|---------------------------|---------------------------|-------------|
| 60 | 0.032 at $V_{GS} = 10$ V | 50 | 66 nC |
| | 0.035 at $V_{GS} = 4.5$ V | 40 | |

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Logic-Level Gate Drive
- Fast Switching
- Compliant to RoHS Directive 2002/95/EC



RoHS*
COMPLIANT
HALOGEN
FREE
Available



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

| PARAMETER | | | SYMBOL | LIMIT | UNIT |
|---|-------------------------|-------------------------|-----------------------------------|------------------|------|
| Drain-Source Voltage | | | V _{DS} | 60 | V |
| Gate-Source Voltage | | | V _{GS} | ± 10 | |
| Continuous Drain Current ^f | V _{GS} at 10 V | T _C = 25 °C | I _D | 50 | A |
| Continuous Drain Current | | T _C = 100 °C | | 36 | |
| Pulsed Drain Current ^a | | | I _{DM} | 200 | |
| Linear Derating Factor | | | | 1.0 | W/°C |
| Linear Derating Factor (PCB Mount) ^e | | | | 0.025 | |
| Single Pulse Avalanche Energy ^b | | | E _{AS} | 400 | mJ |
| Maximum Power Dissipation | T _C = 25 °C | | P _D | 150 | W |
| Maximum Power Dissipation (PCB Mount) ^e | T _A = 25 °C | | | 3.7 | |
| Peak Diode Recovery dV/dt ^c | | | dV/dt | 4.5 | V/ns |
| Operating Junction and Storage Temperature Range | | | T _J , T _{stg} | - 55 to + 175 | °C |
| Soldering Recommendations (Peak Temperature) ^d | for 10 s | | | 300 ^d | |

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25$ V, starting $T_J = 25^\circ\text{C}$, $L = 179$ μH , $R_g = 25$ Ω , $I_{AS} = 51$ A (see fig. 12).
- $I_{SD} \leq 51$ A, $dI/dt \leq 250$ A/ μs , $V_{DD} \leq V_{DS}$, $T_J \leq 175^\circ\text{C}$.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).
- Current limited by the package, (die current = 51 A).

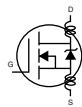

THERMAL RESISTANCE RATINGS

| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
|--|------------|------|------|------|
| Maximum Junction-to-Ambient | R_{thJA} | - | 62 | °C/W |
| Maximum Junction-to-Ambient (PCB Mount) ^a | R_{thJA} | - | 40 | |
| Maximum Junction-to-Case (Drain) | R_{thJC} | - | 1.0 | |

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---------------------|--|--|------|-------|-----------------|-----------------------|
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0$, $I_D = 250\text{ }\mu\text{A}$ | | 60 | - | - | V |
| V_{DS} Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to $25\text{ }^{\circ}\text{C}$, $I_D = 1\text{ mA}$ | | - | 0.070 | - | V/ $^{\circ}\text{C}$ |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$ | | 1.0 | - | 3.0 | V |
| Gate-Source Leakage | I_{GSS} | $V_{GS} = \pm 10\text{ V}$ | | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 60\text{ V}$, $V_{GS} = 0\text{ V}$ | | - | - | 25 | μA |
| | | $V_{DS} = 48\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 150\text{ }^{\circ}\text{C}$ | | - | - | 250 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$ | $I_D = 21\text{ A}^b$ | - | 0.032 | - | Ω |
| | | $V_{GS} = 4.5\text{ V}$ | $I_D = 15\text{ A}^b$ | - | 0.035 | - | |
| Forward Transconductance | g_{fs} | $V_{DS} = 25\text{ V}$, $I_D = 21\text{ A}^b$ | | 23 | - | - | S |
| Dynamic | | | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5 | | - | 3000 | - | pF |
| Output Capacitance | C_{oss} | | | - | 1000 | - | |
| Reverse Transfer Capacitance | C_{rss} | | | - | 200 | - | |
| Total Gate Charge | Q_g | $V_{GS} = 5.0\text{ V}$ | $I_D = 51\text{ A}$, $V_{DS} = 48\text{ V}$, see fig. 6 and 13 ^b | - | 60 | - | nC |
| Gate-Source Charge | Q_{gs} | | | - | 10 | - | |
| Gate-Drain Charge | Q_{gd} | | | - | 40 | - | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 30\text{ V}$, $I_D = 51\text{ A}$, $R_g = 4.6\text{ }\Omega$, $R_D = 0.56\text{ }\Omega$, see fig. 10 ^b | | - | 17 | - | ns |
| Rise Time | t_r | | | - | 230 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | - | 42 | - | |
| Fall Time | t_f | | | - | 110 | - | |
| Internal Drain Inductance | L_D | Between lead, 6 mm (0.25") from package and center of die contact  | | - | 4.5 | - | nH |
| Internal Source Inductance | L_S | | | - | 7.5 | - | |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous Source-Drain Diode Current | I_S | MOSFET symbol showing the integral reverse p - n junction diode  | | - | - | 50 ^c | A |
| Pulsed Diode Forward Current ^a | I_{SM} | | | - | - | 200 | |
| Body Diode Voltage | V_{SD} | $T_J = 25\text{ }^{\circ}\text{C}$, $I_S = 51\text{ A}$, $V_{GS} = 0\text{ V}^b$ | | - | - | 2.5 | V |
| Body Diode Reverse Recovery Time | t_{rr} | $T_J = 25\text{ }^{\circ}\text{C}$, $I_F = 51\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}^b$ | | - | 130 | 180 | ns |
| Body Diode Reverse Recovery Charge | Q_{rr} | | | - | 0.84 | 1.3 | μC |
| Forward Turn-On Time | t_{on} | Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D) | | | | | |

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

c. Current limited by the package, (Die Current = 51 A).

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

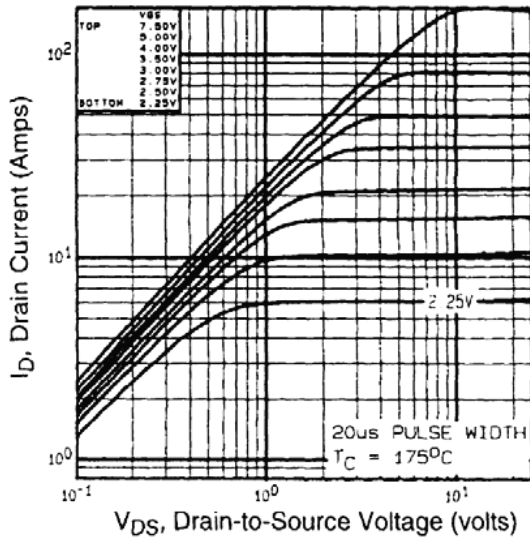




Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



Fig. 7 - Typical Source-Drain Diode Forward Voltage



Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



Fig. 8 - Maximum Safe Operating Area



Fig. 9 - Maximum Drain Current vs. Case Temperature

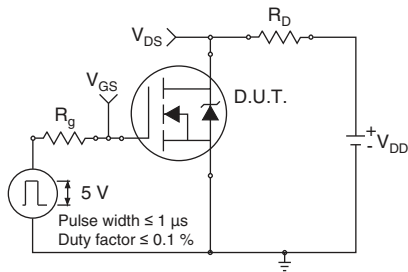


Fig. 10a - Switching Time Test Circuit

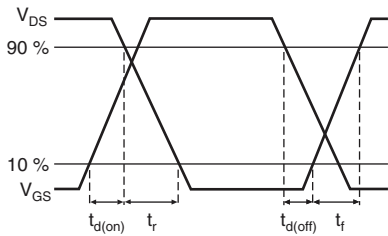


Fig. 10b - Switching Time Waveforms

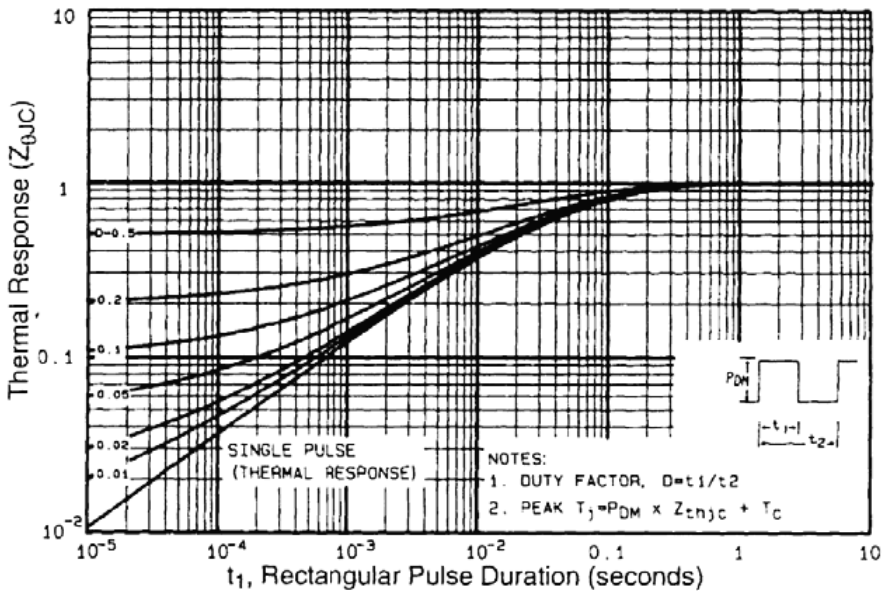


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



Fig. 12a - Unclamped Inductive Test Circuit



Fig. 12b - Unclamped Inductive Waveforms



Fig. 12c - Maximum Avalanche Energy vs. Drain Current

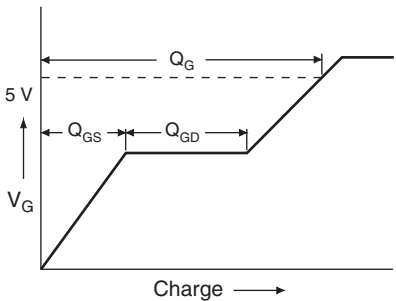


Fig. 13a - Basic Gate Charge Waveform



Fig. 13b - Gate Charge Test Circuit



Note

a. $V_{GS} = 5V$ for logic level devices

Fig. 14 - For N-Channel

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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