

# IRFZ24VSPBF-VB Datasheet N-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A) <sup>a, e</sup>	Q <sub>g</sub> (Max)			
60	$0.032 \text{ at V}_{GS} = 10 \text{ V}$	50	66 nC			
	0.035 at V <sub>GS</sub> = 4.5 V	40	00 110			

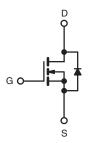
#### **FEATURES**

- Halogen-free According to IEC 61249-2-21 Definition
- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Logic-Level Gate Drive
- Fast Switching
- Compliant to RoHS Directive 2002/95/EC









N-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER			SYMBOL	LIMIT	UNIT		
Drain-Source Voltage	V <sub>DS</sub>	60	V				
Gate-Source Voltage	$V_{GS}$	± 10					
Continuous Drain Current <sup>f</sup>	V <sub>GS</sub> at 10 V	$T_{\rm C} = 25  ^{\circ}{\rm C}$ $T_{\rm C} = 100  ^{\circ}{\rm C}$	l <sub>D</sub>	50			
Continuous Drain Current	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 100 °C		36	Α		
Pulsed Drain Current <sup>a</sup>			I <sub>DM</sub>	200	1		
Linear Derating Factor				1.0	W/°C		
Linear Derating Factor (PCB Mount)e		0.025	VV/ C				
Single Pulse Avalanche Energy <sup>b</sup>	E <sub>AS</sub>	400	mJ				
Maximum Power Dissipation	T <sub>C</sub> = 25 °C		р	150	W		
Maximum Power Dissipation (PCB Mount)e	on (PCB Mount) <sup>e</sup> T <sub>A</sub> =		$P_{D}$	3.7			
Peak Diode Recovery dV/dt <sup>c</sup>			dV/dt	4.5	V/ns		
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 175	°C				
Soldering Recommendations (Peak Temperature) <sup>d</sup>		10 s	-	300 <sup>d</sup>			

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11). b.  $V_{DD} = 25$  V, starting  $T_J = 25$  °C, L = 179  $\mu$ H,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 51$  A (see fig. 12). c.  $I_{SD} \le 51$  A,  $I_{AS} = 51$

- d. 1.6 mm from case.
- e. When mounted on 1" square PCB (FR-4 or G-10 material).
- f. Current limited by the package, (die current = 51 A).



THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	TYP.	MAX.	UNIT		
Maximum Junction-to-Ambient	R <sub>thJA</sub>	-	62			
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	R <sub>thJA</sub>	R <sub>thJA</sub> - 40		°C/W		
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	-	1.0			

#### Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static		<u> </u>		<u> </u>	<u>L</u>		
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0$ , $I_D = 250 \mu A$		60	-	-	V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.070	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \ \mu A$		1.0	-	3.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 10 V		-	-	± 100	nA
	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V		-	-	25	μΑ
Zero Gate Voltage Drain Current		V <sub>DS</sub> = 48 V	V <sub>DS</sub> = 48 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 150 °C		-	250	
5 . 6 . 6	_	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 21 A <sup>b</sup>	-	0.032	-	Ω
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 15 A <sup>b</sup>	-	0.035	-	
Forward Transconductance	9 <sub>fs</sub>	V <sub>DS</sub> = 25 V, I <sub>D</sub> = 21A b		23	-	-	S
Dynamic						l.	
Input Capacitance	C <sub>iss</sub>	$V_{GS} = 0 \text{ V},$ $V_{DS} = 25 \text{ V},$ $f = 1.0 \text{ MHz}, \text{ see fig. } 5$		-	3000	-	pF
Output Capacitance	C <sub>oss</sub>			-	1000	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	200	-	
Total Gate Charge	Qg			-	60	-	nC
Gate-Source Charge	Q <sub>gs</sub>	V <sub>GS</sub> = 5.0 V	$I_D = 51 \text{ A}, V_{DS} = 48 \text{ V},$ see fig. 6 and $13^b$	-	10	-	
Gate-Drain Charge	Q <sub>gd</sub>	See lig. 0 and 15"		-	40	-	
Turn-On Delay Time	t <sub>d(on)</sub>			-	17	-	
Rise Time	t <sub>r</sub>	$V_{DD} = 30 \text{ V}, I_D = 51 \text{ A},$		-	230	-	- ns
Turn-Off Delay Time	t <sub>d(off)</sub>	$R_g = 4.6 \Omega, R_D = 0.56 \Omega, \text{ see fig. } 10^b$		-	42	-	
Fall Time	t <sub>f</sub>	1		-	110	-	
Internal Drain Inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	الم
Internal Source Inductance	L <sub>S</sub>			-	7.5	-	- nH
<b>Drain-Source Body Diode Characteristic</b>	s						
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the		-	-	50°	Α
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>	integral reverse p - n junction diode		-	-	200	
Body Diode Voltage	$V_{SD}$	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 51 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	2.5	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 51 A, dl/dt = 100 A/µs <sup>b</sup>		-	130	180	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	0.84	1.3	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-		on is dor	dominated by L <sub>S</sub> and L <sub>D</sub> )		

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
  b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.
  c. Current limited by the package, (Die Current = 51 A).



#### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

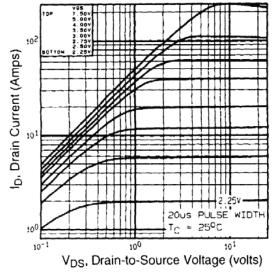


Fig. 1 - Typical Output Characteristics,  $T_C = 25$  °C

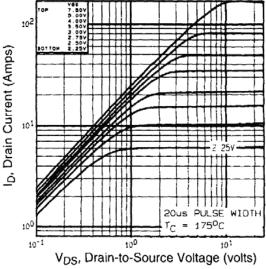


Fig. 2 - Typical Output Characteristics,  $T_C = 150 \, ^{\circ}\text{C}$ 

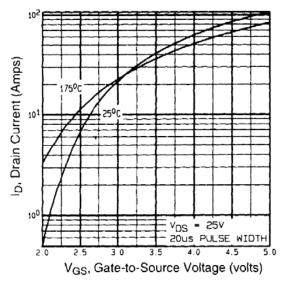


Fig. 3 - Typical Transfer Characteristics

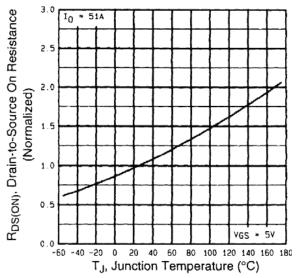


Fig. 4 - Normalized On-Resistance vs. Temperature



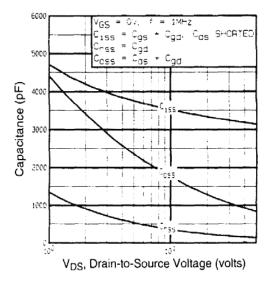


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

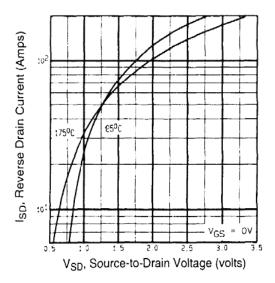


Fig. 7 - Typical Source-Drain Diode Forward Voltage

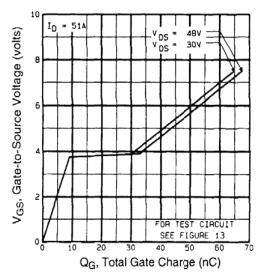


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

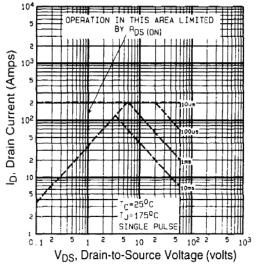


Fig. 8 - Maximum Safe Operating Area



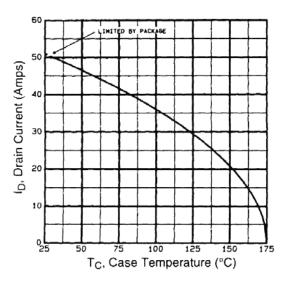


Fig. 9 - Maximum Drain Current vs. Case Temperature

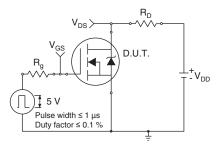


Fig. 10a - Switching Time Test Circuit

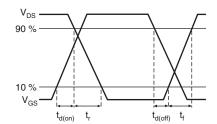


Fig. 10b - Switching Time Waveforms

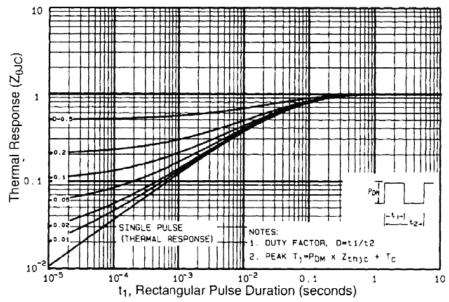
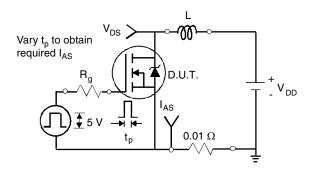


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

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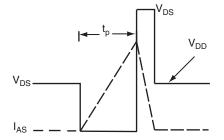


Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

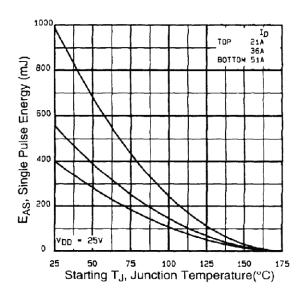


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

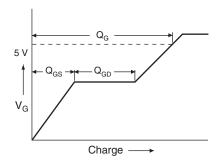


Fig. 13a - Basic Gate Charge Waveform

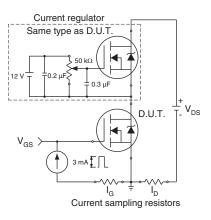
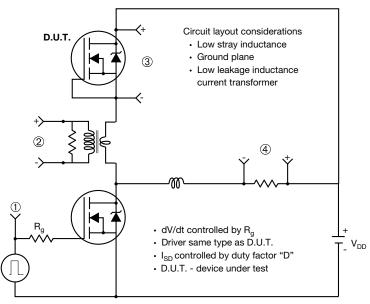


Fig. 13b - Gate Charge Test Circuit



#### Peak Diode Recovery dV/dt Test Circuit



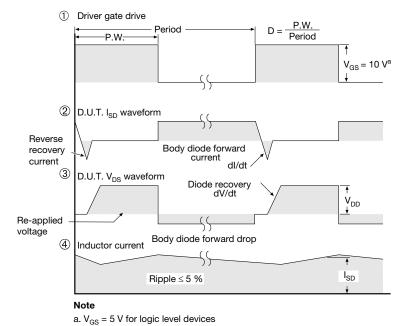
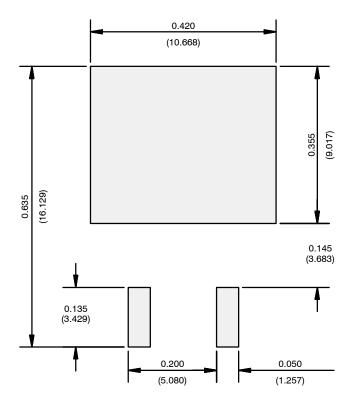


Fig. 14 - For N-Channel



### RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)



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