

## IRF9530STRR-VB Datasheet

### P-Channel 100 V (D-S) MOSFET

#### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ ) Max.	$I_D$ (A)	$Q_g$ (Typ.)
-100	0.22 at $V_{GS} = -10$ V	-12	67
	0.24 at $V_{GS} = -4.5$ V	-10	

#### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Trench Power MOSFET
- 100 %  $R_g$  and UIS Tested
- Compliant to RoHS Directive 2002/95/EC

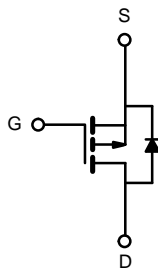
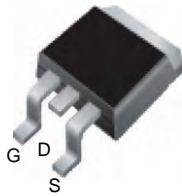


**RoHS**  
COMPLIANT

#### APPLICATIONS

- Power Switch
- Load Switch in High Current Applications
- DC/DC Converters

D<sup>2</sup>PAK (TO-263)



P-Channel MOSFET

#### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ , unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ )	$I_D$	$T_C = 25^\circ\text{C}$ -12	A
		$T_C = 70^\circ\text{C}$ -10	
Pulsed Drain Current ( $t = 300\ \mu\text{s}$ )	$I_{DM}$	-40	
Avalanche Current	$I_{AS}$	-32	
Single Avalanche Energy <sup>a</sup>	$E_{AS}$	51	mJ
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_C = 25^\circ\text{C}$ 50.7 <sup>b</sup>	W
		$T_A = 25^\circ\text{C}^c$ 2.1	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

#### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mount) <sup>c</sup>	$R_{thJA}$	60	$^\circ\text{C}/\text{W}$
Junction-to-Case (Drain)	$R_{thJC}$	3	

Notes:

- Duty cycle  $\leq 1\%$ .
- See SOA curve for voltage derating.
- When mounted on 1" square PCB (FR-4 material).

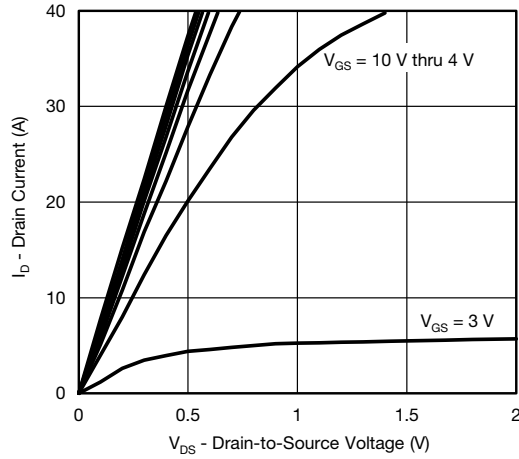
SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>DS</sub> = 0 V, I <sub>D</sub> = - 250 μA	- 100			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = - 250 μA	- 1		- 3.0	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 250	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = - 100V, V <sub>GS</sub> = 0 V			- 1	μA
		V <sub>DS</sub> = - 100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			- 50	
		V <sub>DS</sub> = - 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 150 °C			- 250	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ - 10 V, V <sub>GS</sub> = - 10 V	- 30			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 14 A		0.22		Ω
		V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 12 A		0.24		
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = - 20 V, I <sub>D</sub> = - 14 A		40		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = - 20 V, f = 1 MHz		2765		pF
Output Capacitance	C <sub>oss</sub>			330		
Reverse Transfer Capacitance	C <sub>rss</sub>			280		
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 14 A		67		nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			13.5		
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			14		
Gate Resistance	R <sub>g</sub>	f = 1 MHz	0.5	2.5	5	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = - 20 V, R <sub>L</sub> = 2 Ω I <sub>D</sub> ≅ - 10 A, V <sub>GEN</sub> = - 10 V, R <sub>g</sub> = 1 Ω		10	20	ns
Rise Time <sup>c</sup>	t <sub>r</sub>			11	20	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			42	63	
Fall Time <sup>c</sup>	t <sub>f</sub>			12	20	
Drain-Source Body Diode Ratings and Characteristics T <sub>C</sub> = 25 °C <sup>b</sup>						
Continuous Current	I <sub>S</sub>				- 36	A
Pulsed Current	I <sub>SM</sub>				- 100	
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = - 10 A, V <sub>GS</sub> = 0 V		- 0.8	- 1.5	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = - 10 A, dI/dt = 100 A/μs		38	57	ns
Peak Reverse Recovery Current	I <sub>RM(REC)</sub>			2.3	3.5	A
Reverse Recovery Charge	Q <sub>rr</sub>			40	60	nC

Notes:

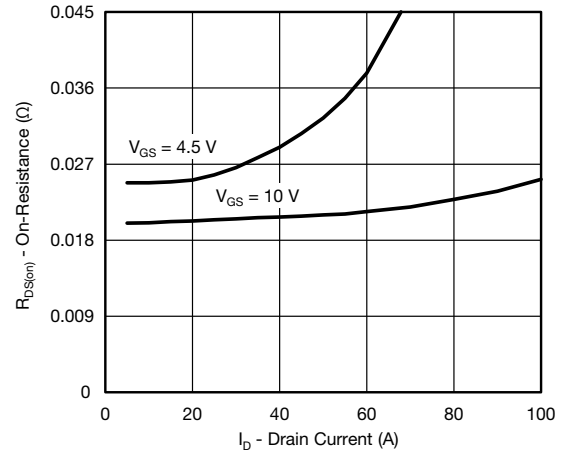
- Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

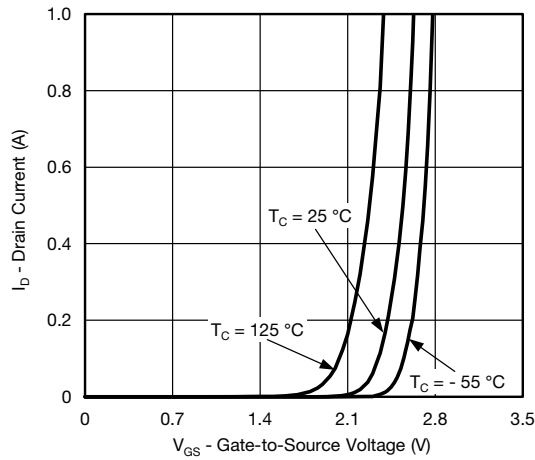
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



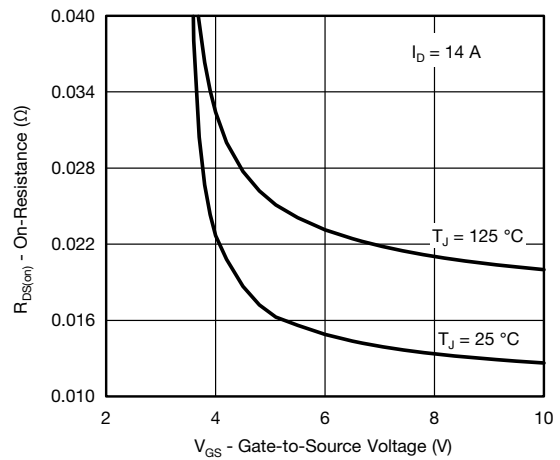
**Output Characteristics**



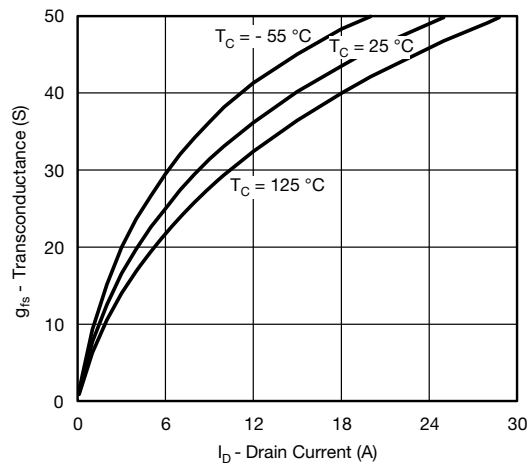
**On-Resistance vs. Drain Current**



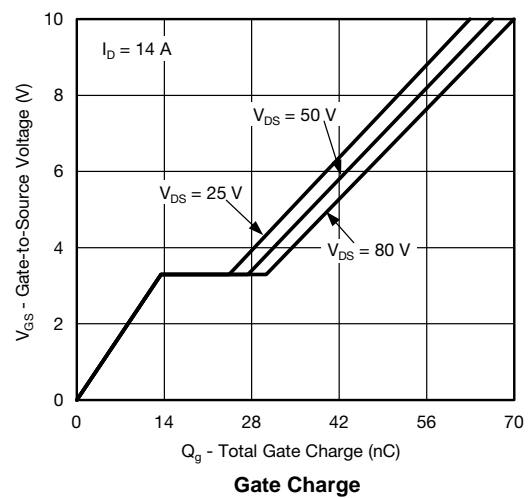
**Transfer Characteristics**



**On-Resistance vs. Gate-to-Source Voltage**

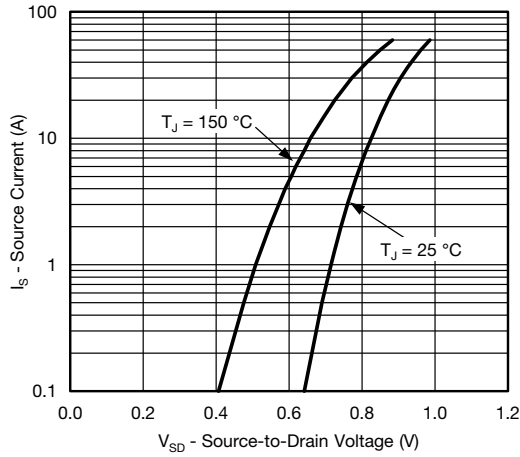


**Transconductance**

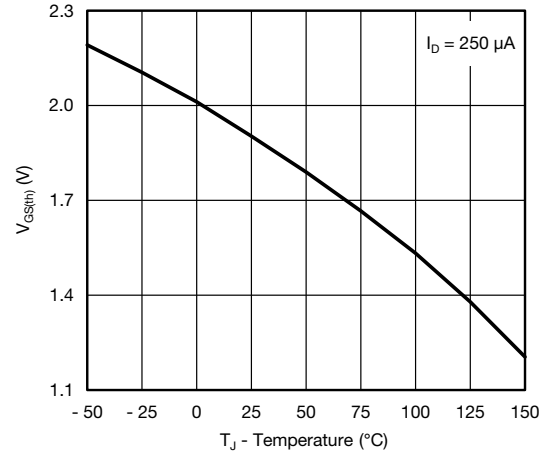


**Gate Charge**

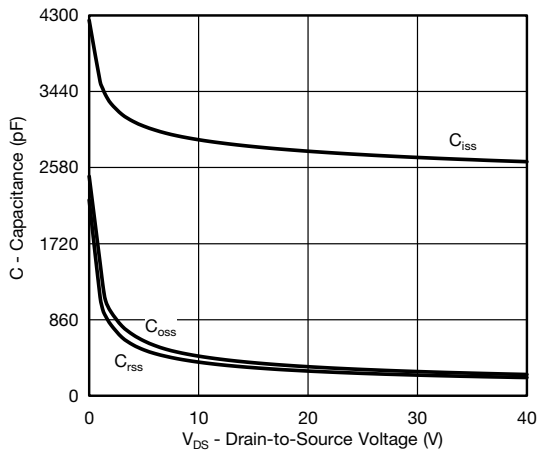
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



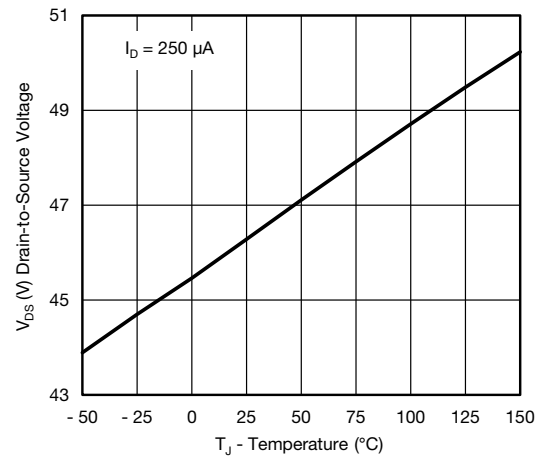
Source-Drain Diode Forward Voltage



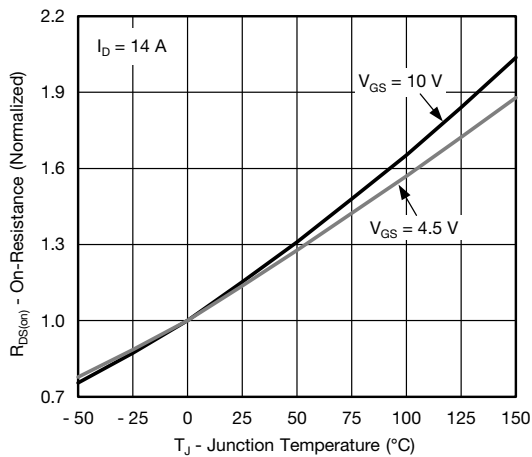
Threshold Voltage



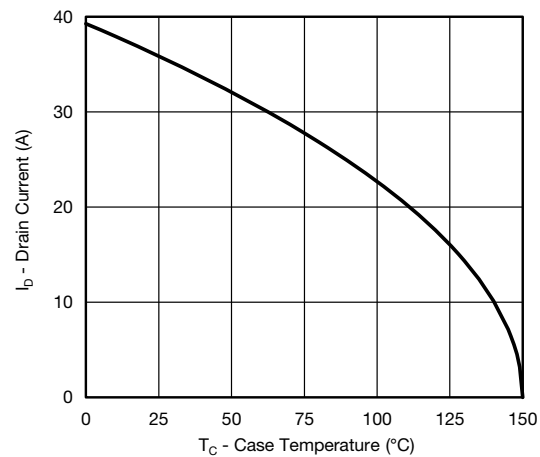
Capacitance



Drain Source Breakdown vs. Junction Temperature

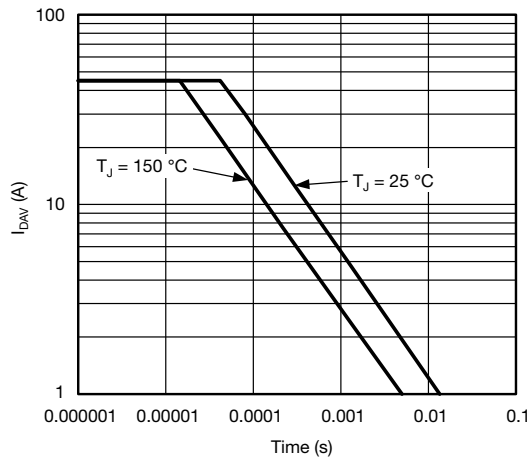


On-Resistance vs. Junction Temperature

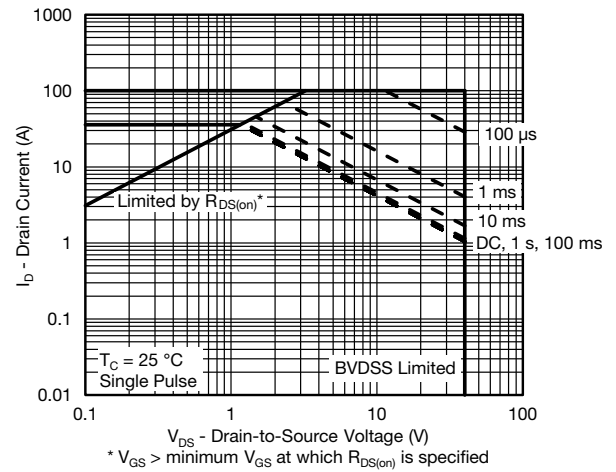


Current Derating

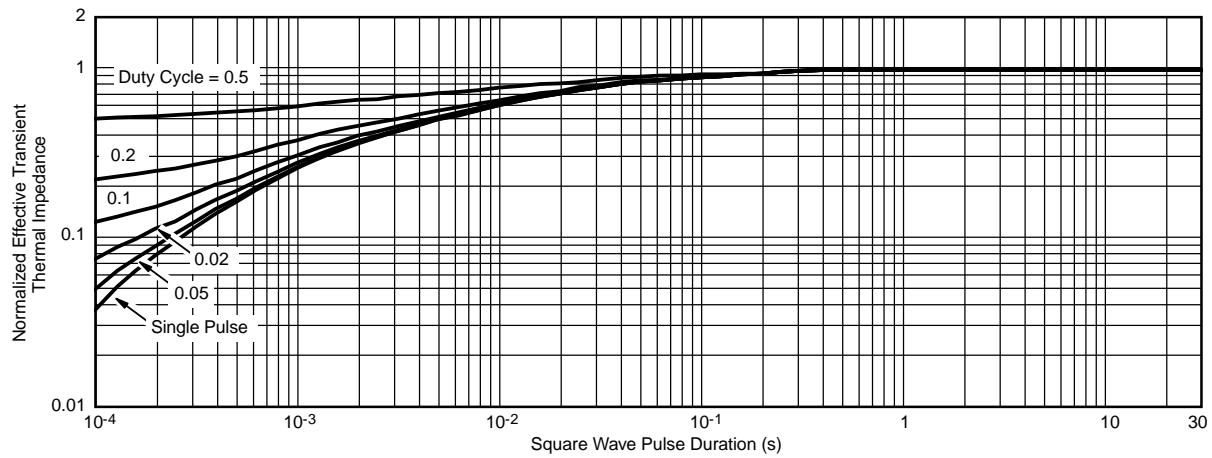
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



Single Pulse Avalanche Current Capability vs. Time

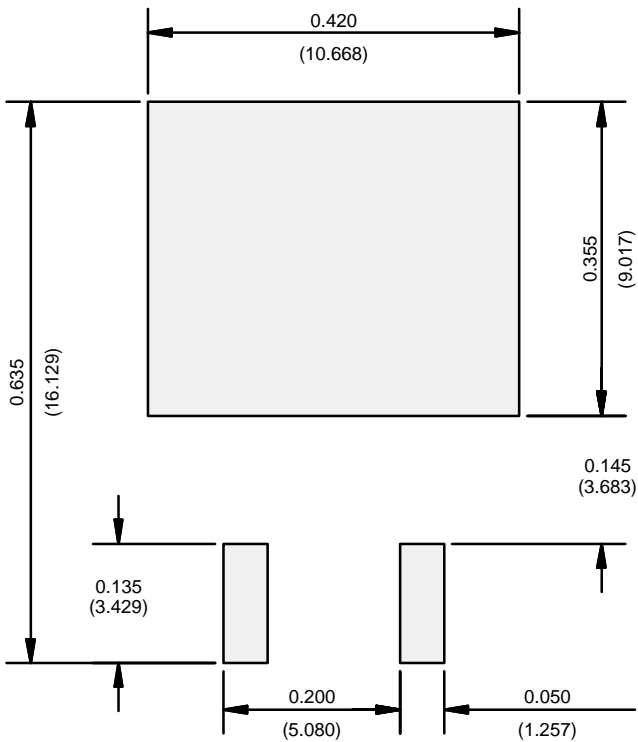


Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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