

IRF3315STRLPBF-VB Datasheet N-Channel 150V (D-S) MOSFET

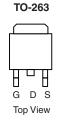
PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)			
150	0.035 at V _{GS} = 10 V	45			
130	0.042 at V _{GS} = 7.5 V	42			

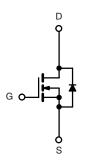
FEATURES

- Trench Power MOSFETs
- 175 °C Junction Temperature
- New Low Thermal Resistance Package
- PWM Optimized
- Compliant to RoHS Directive 2002/95/EC



· Primary Side Switch





N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	i T _C = 25 °C, unless oth	erwise noted			
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage		V _{DS}	150	V	
Gate-Source Voltage		V _{GS}	± 20	_ v	
Continuous Drain Current (T _{.1} = 175 °C)	T _C = 25 °C	I-	45		
Continuous Diam Current (1j = 175 C)	T _C = 125 °C	I _D	31	_	
Pulsed Drain Current		I _{DM}	140	A	
Avalanche Current		I _{AR}	50		
Repetitive Avalanche Energy ^a	L = 0.1 mH	E _{AR}	80	mJ	
	T _C = 25 °C	В	160 ^b	14/	
Maximum Power Dissipation ^a	T _A = 25 °C ^c	$ P_D$ $-$	3.7	W	
Operating Junction and Storage Temperature Range		T _J , T _{sta}	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Limit	Unit	
Junction-to-Ambient (PCB Mount TO-263 ^c)	R _{thJA}	40	°C/W	
Junction-to-Case (Drain)	R _{thJC}	0.9	C/VV	

Notes:

- a. Duty cycle \leq 1 %.
- b. See SOA curve for voltage derating.
- c. When Mounted on 1" square PCB (FR-4 material).



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{DS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	150			V	
Gate-Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	4		6	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
		V _{DS} = 150 V, V _{GS} = 0 V			1		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 120 V, V _{GS} = 0 V, T _J = 125 °C			50	μΑ	
		V _{DS} = 120 V, V _{GS} = 0 V, T _J = 175 °C			250		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	80			Α	
		V _{GS} = 10 V, I _D = 15 A		0.035		Ω	
5		V _{GS} = 7.5 V, I _D = 10 A		0.042			
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 15 A, T _J = 125 °C		0.060			
		V _{GS} = 10 V, I _D = 15 A, T _J = 175 °C		0.080			
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 15 A	10			S	
Dynamic ^b	\						
Input Capacitance	C _{iss}			2200		pF	
Output Capacitance	C _{oss}	$V_{GS} = 0 \text{ V}, V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$		290			
Reverse Transfer Capacitance	C _{rss}			190			
Gate Resistance	Rq			2		Ω	
Total Gate Charge ^c	Qq			38	60		
Gate-Source Charge ^c	Q _{gs}	$V_{DS} = 75 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 40 \text{ A}$		13		nC	
Gate-Drain Charge ^c	Q _{gd}			13			
Turn-On Delay Time ^c	t _{d(on)}			15	25		
Rise Time ^c	t _r	$V_{DD} = 75 \text{ V}, R_1 = 1.80 \Omega$		130	200		
Turn-Off Delay Time ^c	t _{d(off)}	$I_D \cong 40 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 2.5 \Omega$		30	45	ns	
Fall Time ^c	t _f	_		90	140		
Source-Drain Diode Ratings and Cha	racteristics	Γ _C = 25 °C ^b		<u> </u>			
Continuous Current	I _S				40		
Pulsed Current	I _{SM}				80	Α	
Forward Voltage ^a	V _{SD}	I _F = 40 A, V _{GS} = 0 V		1.0	1.5	V	
Reverse Recovery Time	t _{rr}			100	150	ns	
Peak Reverse Recovery Current	I _{RM(REC)}	I _F = 40 A, dl/dt = 100 A/μs		5	8	Α	
Reverse Recovery Charge	Q _{rr}			0.25	0.6	μC	

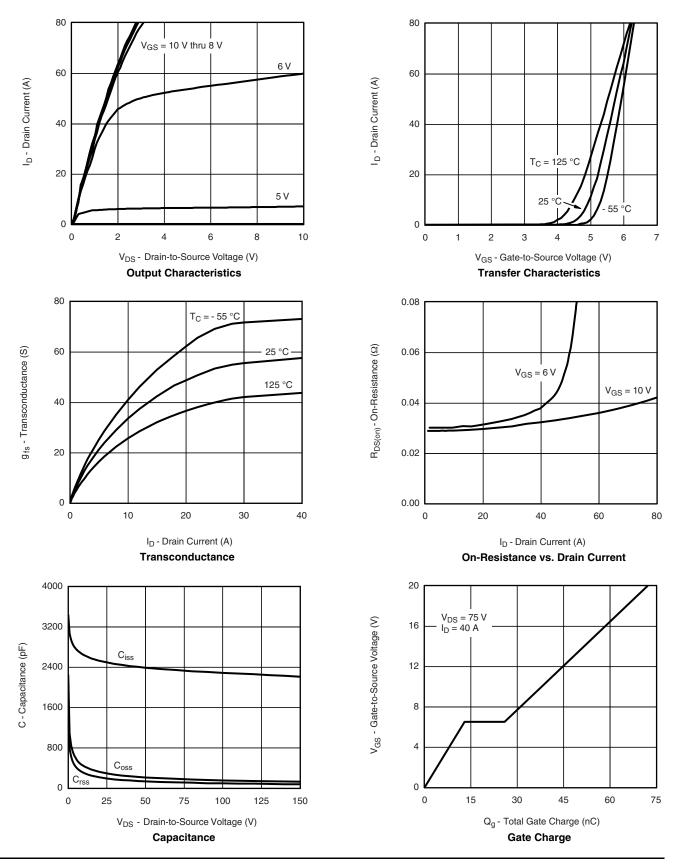
Notes:

- a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 % b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

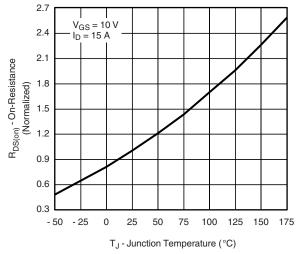


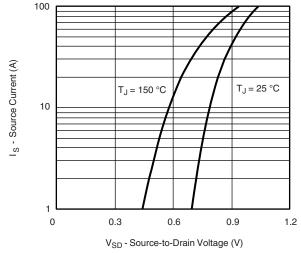
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





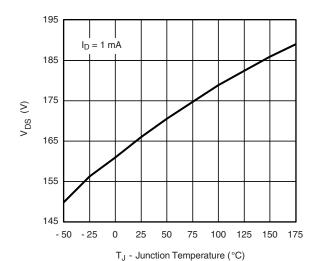
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On-Resistance vs. Junction Temperature

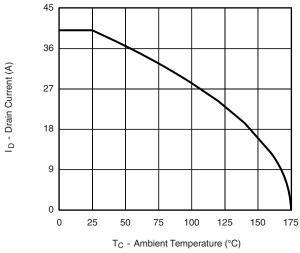
Source-Drain Diode Forward Voltage

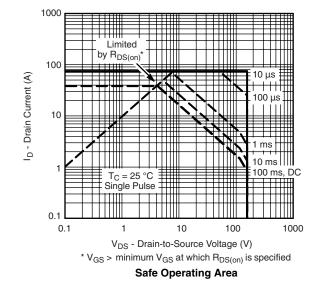


Drain Source Breakdown vs. Junction Temperature

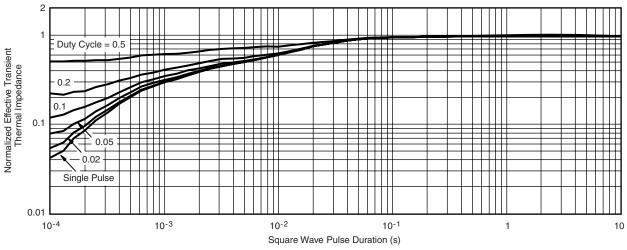


THERMAL RATINGS





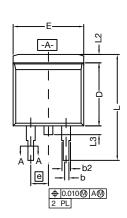
Maximum Avalanche and Drain Current vs. Case Temperature

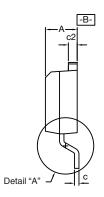


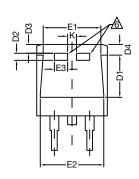
Normalized Thermal Transient Impedance, Junction-to-Case



TO-263 (D²PAK): 3-LEAD

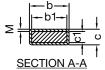








DETAIL A (ROTATED 90°)



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2:			5	ပ
		OTION	1	t

- 1. Plane B includes maximum features of heat sink tab and plastic.
- 2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- 3. Pin-to-pin coplanarity max. 4 mils.
- 4. *: Thin lead is for SUB, SYB. Thick lead is for SUM, SYM, SQM.
- 5. Use inches as the primary measurement.

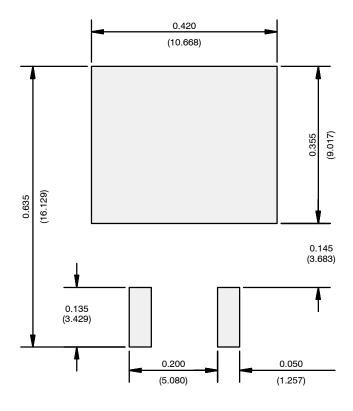
6 This feature is for thick lead.

		INC	HES	MILLIMETERS		
	DIM.	MIN.	MAX.	MIN.	MAX.	
Α		0.160	0.190	4.064	4.826	
	b	0.020	0.039	0.508	0.990	
	b1	0.020	0.035	0.508	0.889	
	b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457	
C	Thick lead	0.023	0.028	0.584	0.711	
c1	Thin lead	0.013	0.017	0.330	0.431	
CI	Thick lead	0.023	0.027	0.584	0.685	
	c2	0.045	0.055	1.143	1.397	
	D	0.340	0.380	8.636	9.652	
	D1	0.220	0.240	5.588	6.096	
	D2	0.038	0.042	0.965	1.067	
	D3	0.045	0.055	1.143	1.397	
	D4	0.044	0.052	1.118	1.321	
	Е	0.380	0.410	9.652	10.414	
	E1	0.245	-	6.223 -		
	E2	0.355	0.375	9.017 9.52		
	E3	0.072	0.078	1.829 1.98		
	е	0.100 BSC		2.54 BSC		
	K	0.045	0.055	1.143	1.397	
	L	0.575	0.625	14.605	15.875	
L1		0.090	0.110	2.286	2.794	
L2		0.040	0.055	1.016	1.397	
L3		0.050	0.070	1.270	1.778	
	L4	0.010 BSC		0.254 BSC		
	М				0.050	
ECN: T13-0707-Rev. K, 30-Sep-13						

DWG: 5843



RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)



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