

# IRF1405STRR-VB Datasheet

## N-Channel 60 V (D-S) MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	60
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 10$ V	0.0028
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 4.5$ V	0.0120
$I_D$ (A)	210
Configuration	Single

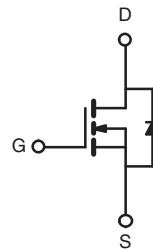
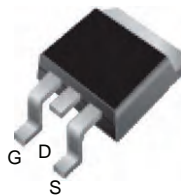
### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Trench Power MOSFET
- Package with Low Thermal Resistance
- 100 %  $R_g$  and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

D<sup>2</sup>PAK (TO-263)



N-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		$V_{DS}$	60	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current	$T_C = 25$ °C	$I_D$	210	A
	$T_C = 125$ °C		120 <sup>a</sup>	
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	120 <sup>a</sup>	
Pulsed Drain Current <sup>b</sup>		$I_{DM}$	480	
Single Pulse Avalanche Current	L = 0.1 mH	$I_{AS}$	75	
Single Pulse Avalanche Energy		$E_{AS}$	281	mJ
Maximum Power Dissipation <sup>b</sup>	$T_C = 25$ °C	$P_D$	375	W
	$T_C = 125$ °C		125	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to + 175	°C

### THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount <sup>c</sup>	$R_{thJA}$	40	°C/W
Junction-to-Case (Drain)		$R_{thJC}$	0.4	

#### Notes

- Package limited.
- Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %.
- When mounted on 1" square PCB (FR-4 material).
- Parametric verification ongoing.

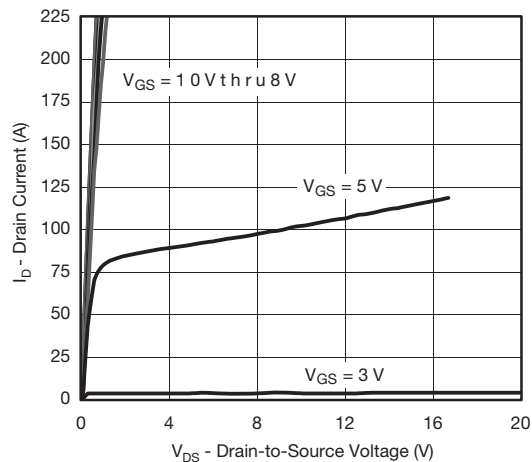
SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0, I <sub>D</sub> = 250 μA		60	-	-	V
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0		4.0	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V	-	-	1.0	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V, T <sub>J</sub> = 125 °C	-	-	50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V, T <sub>J</sub> = 175 °C	-	-	350	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> ≥ 5 V	120	-	-	A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 30 A	-	0.0028	-	Ω
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 30 A, T <sub>J</sub> = 125 °C	-	0.0060	-	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 30 A, T <sub>J</sub> = 175 °C	-	0.0080	-	
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 20 A	-	0.012	-	
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 30 A		-	109	-	S
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 25 V, f = 1 MHz	-	7300	9125	pF
Output Capacitance	C <sub>oss</sub>			-	935	1170	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	647	810	
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 110 A	-	184	276	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			-	24.7	-	
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			-	50.4	-	
Gate Resistance	R <sub>g</sub>	f = 1 MHz		0.5	1.1	1.6	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, R <sub>L</sub> = 0.27 Ω I <sub>D</sub> ≅ 110 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 2.5 Ω		-	19	29	ns
Rise Time <sup>c</sup>	t <sub>r</sub>			-	23	35	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	83	125	
Fall Time <sup>c</sup>	t <sub>f</sub>			-	35	53	
Source-Drain Diode Ratings and Characteristics <sup>b</sup>							
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	480	A
Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> = 100 A, V <sub>GS</sub> = 0		-	0.9	1.5	V

**Notes**

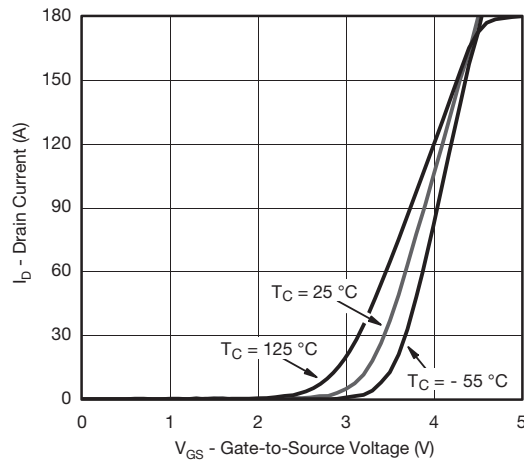
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
 b. Guaranteed by design, not subject to production testing.  
 c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

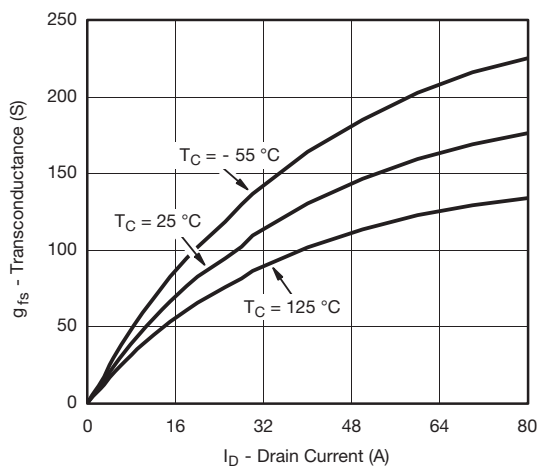
## TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)



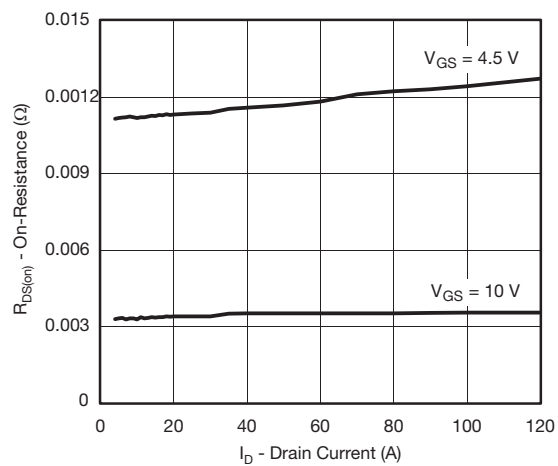
**Output Characteristics**



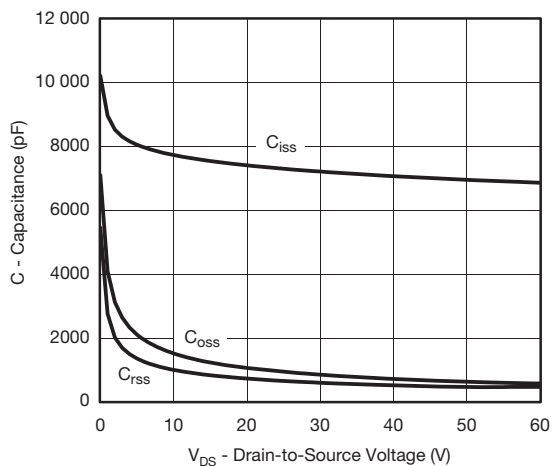
**Transfer Characteristics**



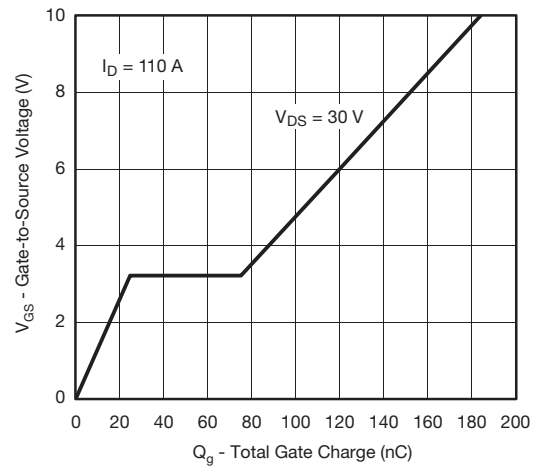
**Transconductance**



**On-Resistance vs. Drain Current**

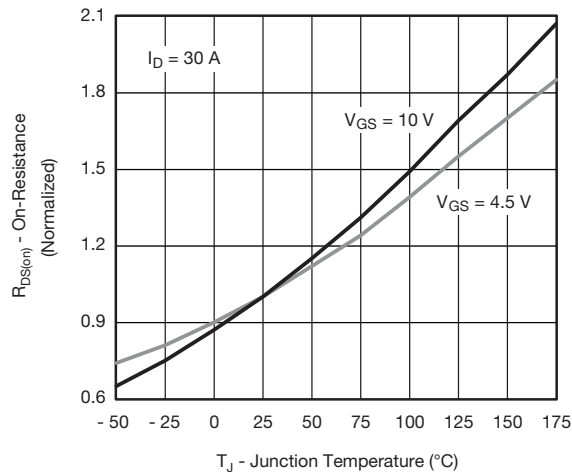


**Capacitance**

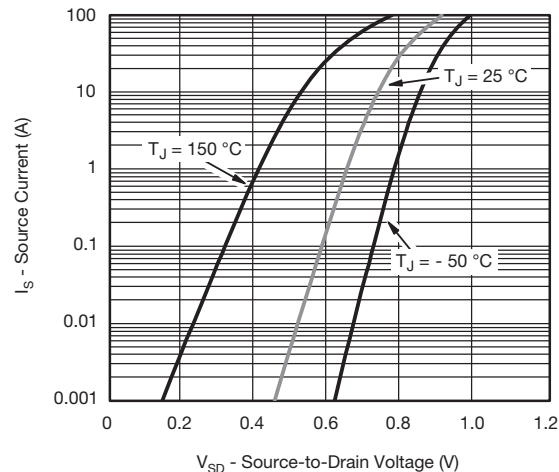


**Gate Charge**

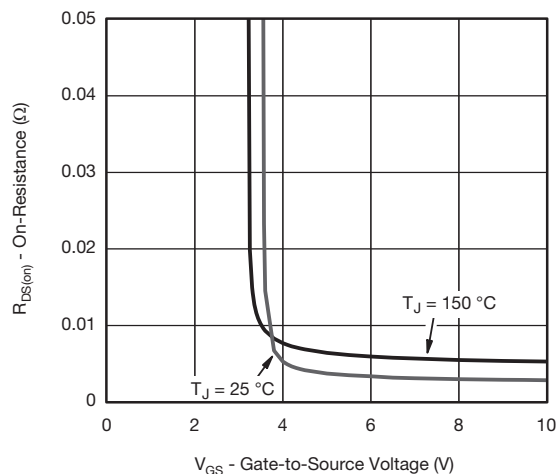
## TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)



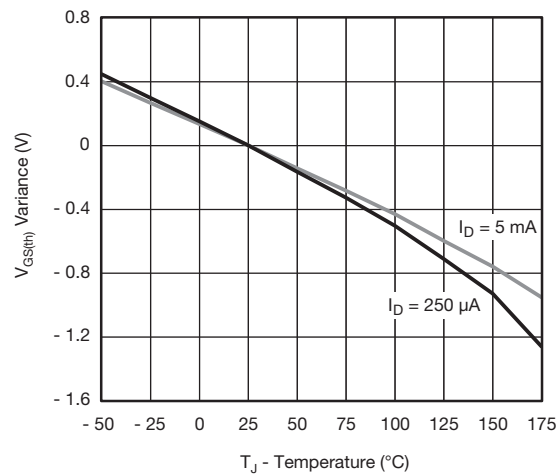
On-Resistance vs. Junction Temperature



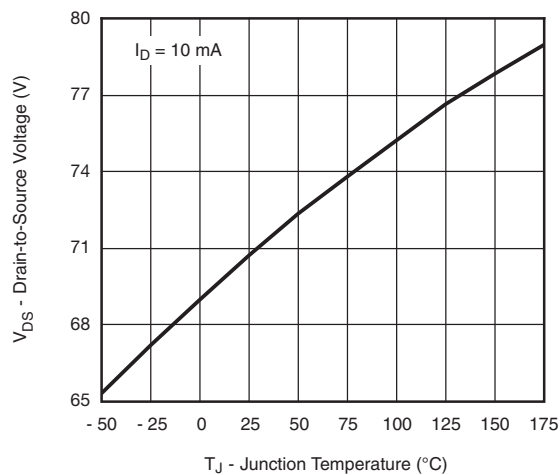
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

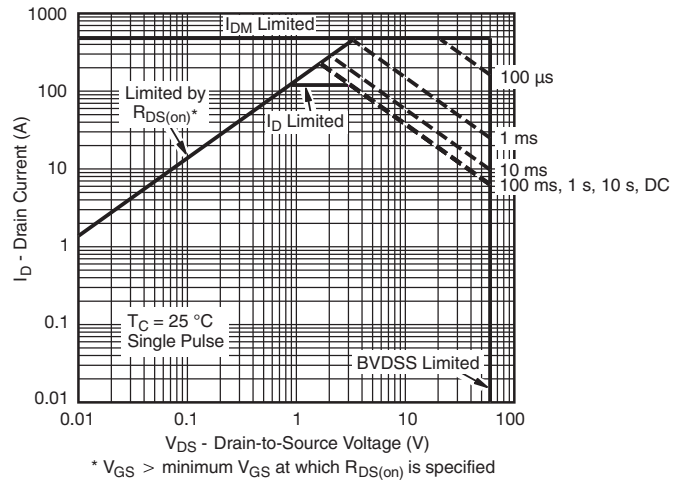


Threshold Voltage

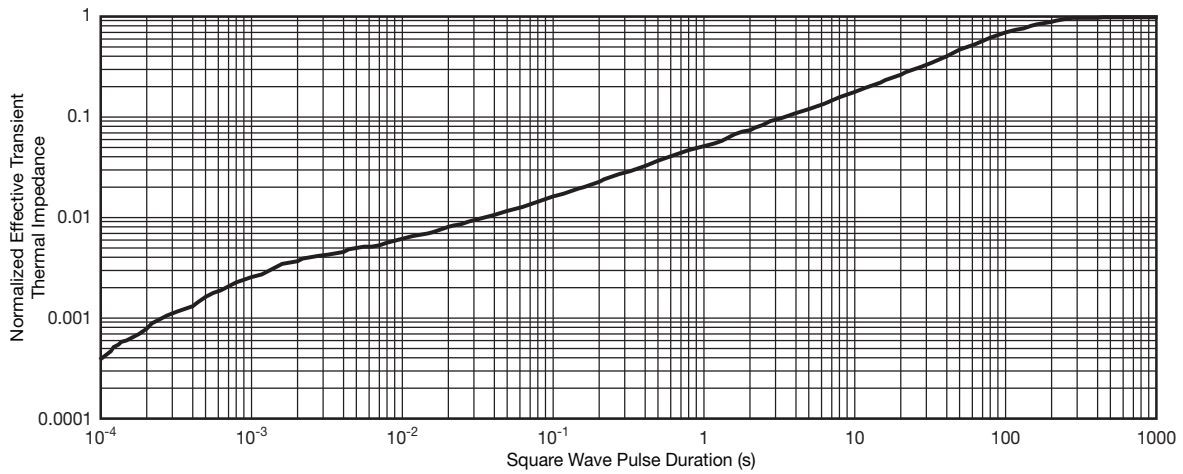


Drain Source Breakdown vs. Junction Temperature

**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

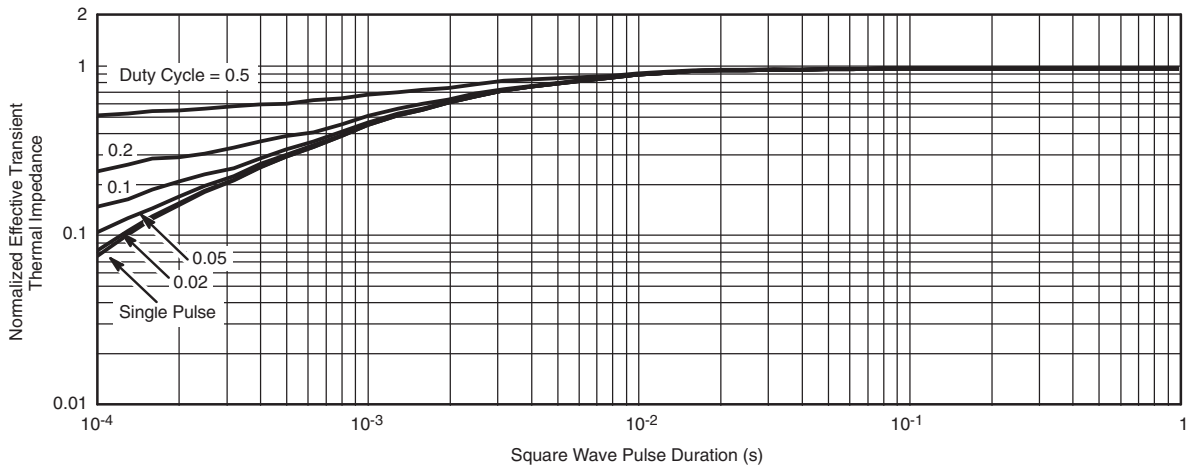


**Safe Operating Area**



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

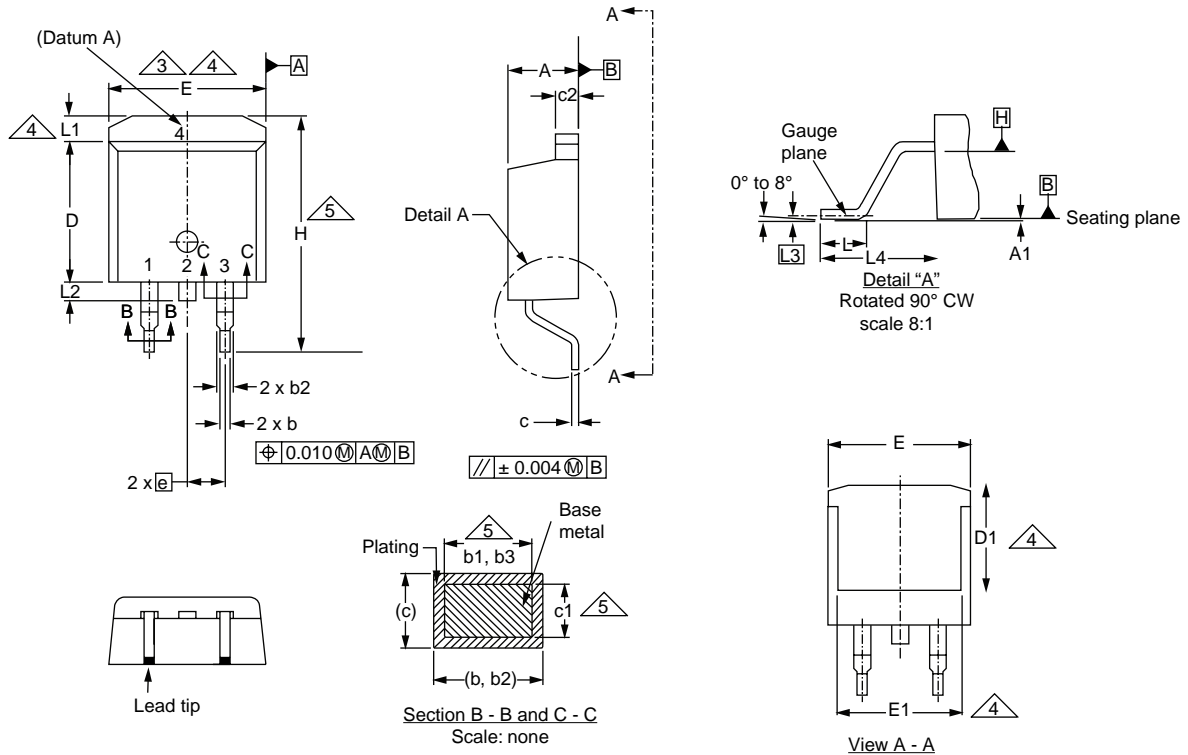


**Normalized Thermal Transient Impedance, Junction-to-Case**

**Note**

- The characteristics shown in the two graphs
    - Normalized Transient Thermal Impedance Junction-to-Ambient ( $25\text{ }^{\circ}\text{C}$ )
    - Normalized Transient Thermal Impedance Junction-to-Case ( $25\text{ }^{\circ}\text{C}$ )
- are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

**TO-263AB**



	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

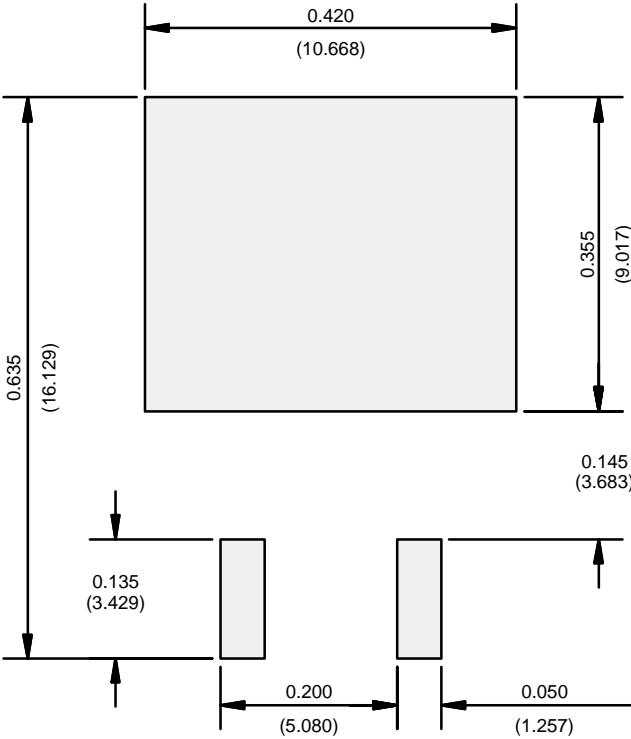
	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08  
DWG: 5970

**Notes**

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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