

# IPB100N06S3-03-VB Datasheet N-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	60			
$R_{DS(on)} (\Omega)$ at $V_{GS} = 10 V$	0.0025			
$R_{DS(on)} (\Omega)$ at $V_{GS} = 4.5 V$	0.0070			
I <sub>D</sub> (A)	270			
Configuration	Single			

## FEATURES

- TrenchFET<sup>®</sup> power MOSFET
- Package with low thermal resistance
- 100 %  $\rm R_g$  and UIS tested





<b>ABSOLUTE MAXIMUM RATINGS</b> ( $T_C = 25 \text{ °C}$ , unless otherwise noted)						
PARAMETER		SYMBOL	LIMIT	UNIT		
Drain-Source Voltage		V <sub>DS</sub>	60	V		
Gate-Source Voltage	V <sub>GS</sub>	± 20				
Continuous Drain Current	T <sub>C</sub> = 25 °C	- I <sub>D</sub>	270			
	T <sub>C</sub> = 125 °C		120 <sup>a</sup>			
Continuous Source Current (Diode Conducti	۱ <sub>S</sub>	120 <sup>a</sup>	A			
Pulsed Drain Current <sup>b</sup>		I <sub>DM</sub>	600			
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	75			
Single Pulse Avalanche Energy	L = 0.1 MH	E <sub>AS</sub>	281	mJ		
Maximum Power Dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C		375	W		
	T <sub>C</sub> = 125 °C		125	vv		
Operating Junction and Storage Temperatur	e Range	T <sub>J</sub> , T <sub>stq</sub>	-55 to +175	°C		

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	LIMIT	UNIT		
Junction-to-Ambient	PCB Mount <sup>c</sup>	R <sub>thJA</sub>	40	°C/W		
Junction-to-Case (Drain)		R <sub>thJC</sub>	0.4	C/W		

#### Notes

a. Package limited.

b. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.

c. When mounted on 1" square PCB (FR4 material).



PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static	<u>.</u>	·					•	
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 V, I_D = 250 \mu A$		60	-	-	v	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$		1.5	2.0	2.5		
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS}$ = 0 V, $V_{GS}$ = ± 20 V		-	-	± 100	nA	
		$V_{GS} = 0 V$	V <sub>DS</sub> = 60 V	-	-	1	μA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 V$	$V_{DS}=60~V,~T_J=125~^\circ C$	-	-	50		
		$V_{GS} = 0 V$	$V_{DS} = 60 \text{ V}, \text{ T}_{J} = 175 ^{\circ}\text{C}$	-	-	1.5	mA	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{GS} = 10 V$	$V_{DS} \ge 5 V$	120	-	-	Α	
		$V_{GS} = 10 V$	I <sub>D</sub> = 30 A	-	0.0025	-		
Drain-Source On-State Resistance <sup>a</sup>	В	$V_{GS} = 10 V$	$I_D = 30 \text{ A},  \text{T}_\text{J} = 125 \ ^\circ\text{C}$	-	0.0040	-	Ω	
Drain-Source On-State Resistance *	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 30 A, T <sub>J</sub> = 175 °C	-	0.0075	-		
		$V_{GS} = 4.5 V$	I <sub>D</sub> = 20 A	-	0.0070	-		
Forward Transconductance b	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 30 A		-	164	-	S	
Dynamic <sup>b</sup>	-							
Input Capacitance	C <sub>iss</sub>			-	9000	-		
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$	V <sub>DS</sub> = 25 V, f = 1 MHz	-	5750	7200	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	860	1100		
Total Gate Charge <sup>c</sup>	Qg			-	128	200	nC	
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	$V_{GS} = 10 V$	$V_{DS} = 30 \text{ V}, \text{ I}_{D} = 80 \text{ A}$	-	33	-		
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>	1		-	11	-		
Gate Resistance	Rg	f = 1 MHz		0.8	1.68	2.6	Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	$V_{DD} = 30 \text{ V}, \text{ R}_{\text{L}} = 0.375 \ \Omega$ $\text{I}_{\text{D}} \cong 80 \text{ A}, \text{ V}_{\text{GEN}} = 10 \text{ V}, \text{ R}_{\text{g}} = 1 \ \Omega$		-	20	25	- ns	
Rise Time <sup>c</sup>	t <sub>r</sub>			-	15	40		
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	65	100		
Fall Time <sup>c</sup>	t <sub>f</sub>	1	-	12	20			
Source-Drain Diode Ratings and Chara	acteristics <sup>b</sup>							
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	200	Α	
Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> = 80 A, V <sub>GS</sub> = 0 V		-	0.88	1.5	V	

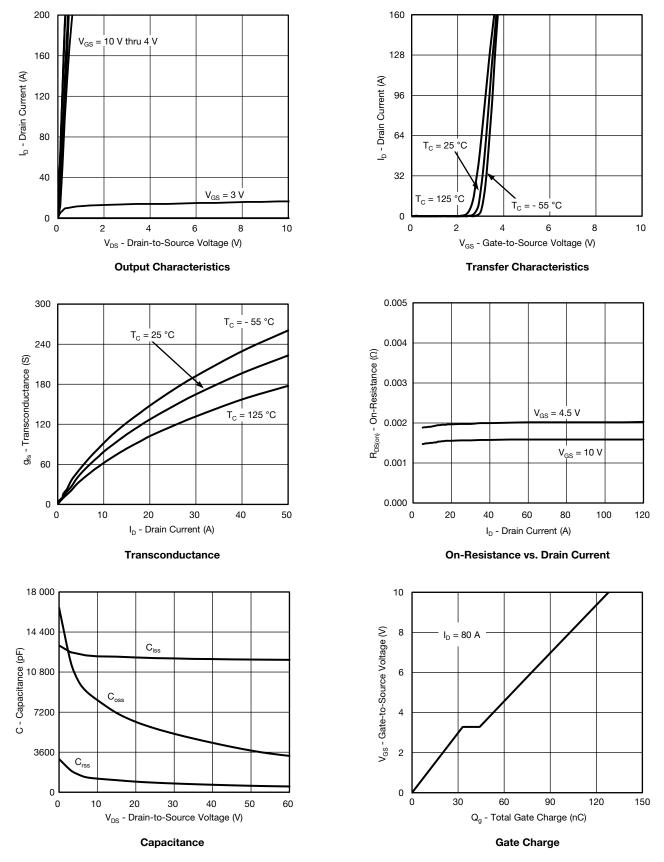
Notes

a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %. b. Guaranteed by design, not subject to production testing.

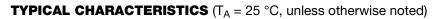
c. Independent of operating temperature.

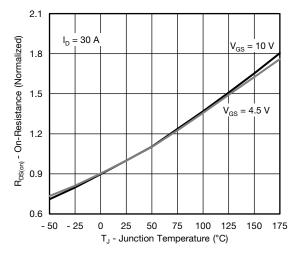


## **TYPICAL CHARACTERISTICS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)

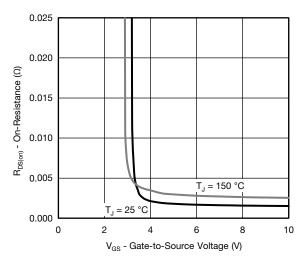




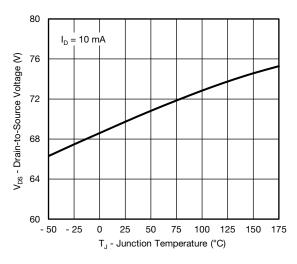




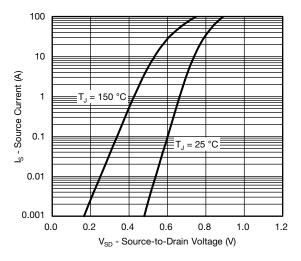
**On-Resistance vs. Junction Temperature** 



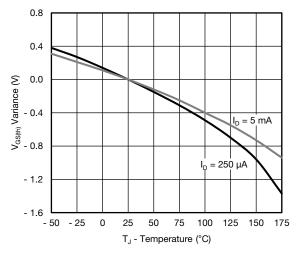
**On-Resistance vs. Gate-to-Source Voltage** 



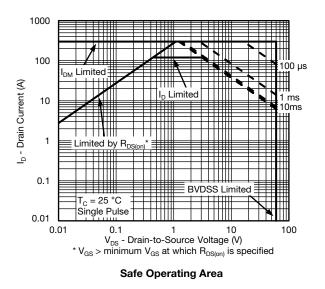
Drain Source Breakdown vs. Junction Temperature



Source Drain Diode Forward Voltage

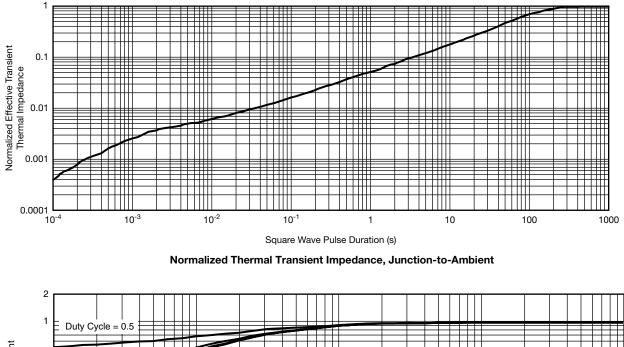


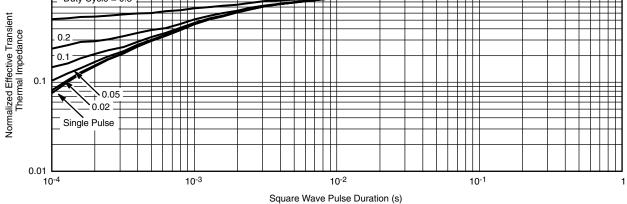


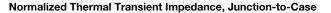




### **THERMAL RATINGS** (T<sub>A</sub> = 25 °C, unless otherwise noted)







#### Note

• The characteristics shown in the two graphs

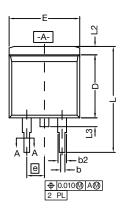
- Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)

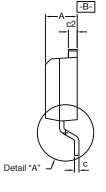
- Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

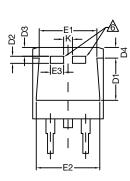
are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.



TO-263 (D<sup>2</sup>PAK): 3-LEAD

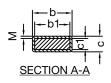








DETAIL A (ROTATED 90°)



		INCHES		MILLIMETERS		
DIM.		MIN.	MAX.	MIN.	MAX.	
А		0.160	0.190	4.064	4.826	
	b	0.020	0.039	0.508	0.990	
	b1	0.020	0.035	0.508	0.889	
b2		0.045	0.045 0.055 1.143		1.397	
с*	Thin lead	0.013	0.018	0.330	0.457	
	Thick lead	0.023	0.028	0.584	0.711	
c1	Thin lead	0.013	0.017	0.330	0.431	
CI	Thick lead	0.023	0.027	0.584	0.685	
c2		0.045	0.055	1.143	1.397	
	D	0.340	0.380	8.636	9.652	
	D1	0.220	0.240	5.588	6.096	
D2		0.038	0.042	0.965	1.067	
D3		0.045	0.055	1.143	1.397	
	D4	0.044	0.052	1.118	1.321	
	E	0.380	0.410	9.652	10.414	
	E1	0.245	-	6.223	-	
	E2	0.355	0.375	9.017	9.525	
	E3	0.072	0.078	0.078 1.829		
	е	0.100	0.100 BSC		BSC	
	К	0.045	0.055	1.143	1.397	
L		0.575	0.625	14.605	15.875	
L1		0.090	0.110	2.286	2.794	
L2		0.040	0.055	1.016	1.397	
L3		0.050	0.070	1.270	1.778	
	L4	0.010 BSC		0.254 BSC		
М		-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13 DWG: 5843						

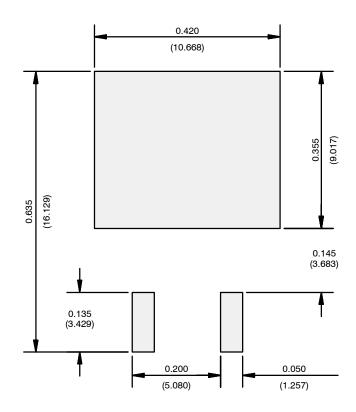
#### Notes

- 1. Plane B includes maximum features of heat sink tab and plastic. 2. No more than 25 % of L1 can fall above seating plane by
- max. 8 mils.3. Pin-to-pin coplanarity max. 4 mils.
- 4. \*: Thin lead is for SUB, SYB.
  - Thick lead is for SUM, SYM, SQM.
- 5. Use inches as the primary measurement.

This feature is for thick lead.



## **RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads Dimensions in Inches/(mm)



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