

# F2907ZS-VB Datasheet N-Channel 80 V (D-S) MOSFET

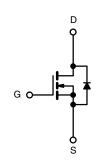
PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}$ ( $\Omega$ ) MAX.	I <sub>D</sub> (A)	Q <sub>g</sub> (TYP.)		
80	0.0050 at V <sub>GS</sub> = 10 V	215	94		
	0.0095 at V <sub>GS</sub> = 7.5 V	205	94		

## **FEATURES**

- Trench power MOSFET
- Maximum 175 °C junction temperature
- Very low Q<sub>gd</sub> reduces power loss from passing through V<sub>plateau</sub>
- 100 % R<sub>g</sub> and UIS tested







N-Channel MOSFET

## **APPLICATIONS**

- Power supply
  - Secondary synchronous rectification
- DC/DC converter
- Power tools
- Motor drive switch
- DC/AC inverter
- Battery management

<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>C</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	LIMIT	UNIT			
Drain-Source Voltage	V <sub>DS</sub>	80	V			
Gate-Source Voltage	V <sub>GS</sub>	± 20	7 v			
Outline - Build Outline   450 00)	T <sub>C</sub> = 25 °C		215			
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>C</sub> = 70 °C	I <sub>D</sub>	120 <sup>d</sup>			
Pulsed Drain Current (t = 100 μs)	I <sub>DM</sub>	600	A			
Avalanche Current	I <sub>AS</sub>	70				
Single Avalanche Energy <sup>a</sup> L = 0.1 mH		E <sub>AS</sub>	245	mJ		
Mayimum Dawar Dissination 3	T <sub>C</sub> = 25 °C	В	375 b	14/		
Maximum Power Dissipation <sup>a</sup>	T <sub>C</sub> = 125 °C	$ P_D$	125 <sup>b</sup>	W		
Operating Junction and Storage Temperature R	T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C			

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	LIMIT	UNIT		
Junction-to-Ambient (PCB Mount) <sup>c</sup>	R <sub>thJA</sub>	40	°C/W		
Junction-to-Case (Drain)	R <sub>thJC</sub>	0.4			

#### Notes

- a. Duty cycle  $\leq$  1 %.
- b. See SOA curve for voltage derating.
- c. When mounted on 1" square PCB (FR4 material).
- d. Package limited.



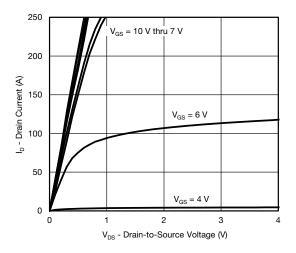
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static			•	•			
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	80	-	-	V	
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$		-	4	V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	± 250	nA	
		V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V	-	-	1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	150	μA	
		V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C	-	-	5	mA	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	120	-	-	Α	
Drain-Source On-State Resistance a	В	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 30 A	-	0.0050	-	Ω	
Drain-Source On-State Resistance 4	R <sub>DS(on)</sub>	V <sub>GS</sub> = 7.5 V, I <sub>D</sub> = 20 A	-	0.0095	-		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 30 A	-	82	-	S	
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 40 V, f = 1 MHz	-	7910	-	pF	
Output Capacitance	C <sub>oss</sub>		-	3250	-		
Reverse Transfer Capacitance	C <sub>rss</sub>		-	348	-		
Total Gate Charge <sup>c</sup>	Qg		-	94	141		
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	$V_{DS} = 40 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$	-	31	-	nC	
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$		-	10	-		
Gate Resistance	$R_g$	f = 1 MHz	0.28	1.4	2.8	Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>		-	24	40		
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = 40 \text{ V}, \text{ R}_{L} = 4 \Omega$	-	24	40		
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	$I_D\cong 10~A,~V_{GEN}=10~V,~R_g=1~\Omega$	-	34	60	ns	
Fall Time <sup>c</sup>	t <sub>f</sub>		-	14	28		
Drain-Source Body Diode Ratings ar	nd Characteris	stics <sup>b</sup> (T <sub>C</sub> = 25 °C)					
Pulsed Current (t = 100 μs)	I <sub>SM</sub>		-	-	250	Α	
Forward Voltage <sup>a</sup>	$V_{SD}$	I <sub>F</sub> = 10 A, V <sub>GS</sub> = 0 V	-	0.8	1.5	V	
Reverse Recovery Time	t <sub>rr</sub>		-	126	190	ns	
Peak Reverse Recovery Charge	I <sub>RM(REC)</sub>	$I_F = 34 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$	-	5	10	Α	
Reverse Recovery Charge	Q <sub>rr</sub>		-	0.315	0.475	иC	

## Notes

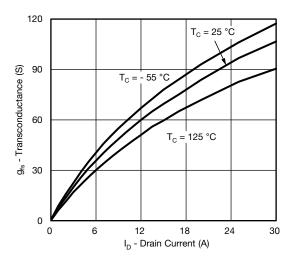
- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %. b. Guaranteed by design, not subject to production testing. c. Independent of operating temperature.



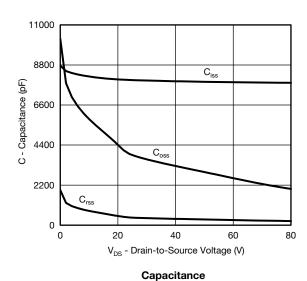
## **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)

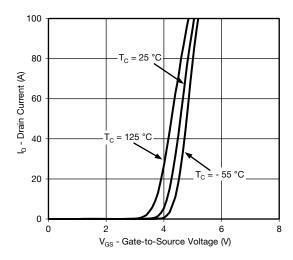


## **Output Characteristics**

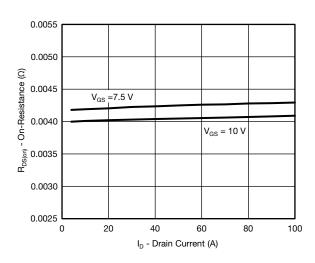


## Transconductance

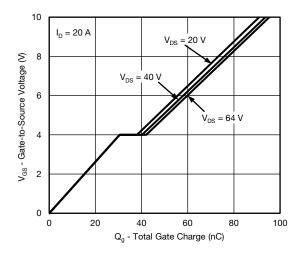




#### **Transfer Characteristics**



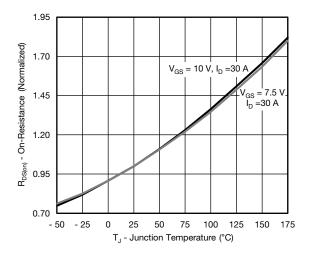
## On-Resistance vs. Drain Current



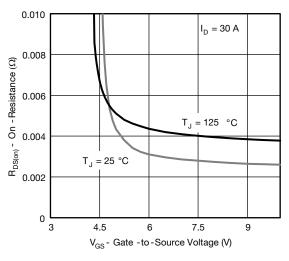
**Gate Charge** 



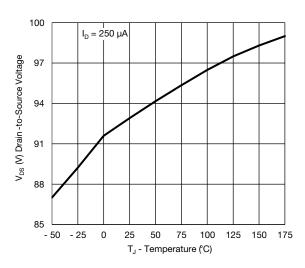
## TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



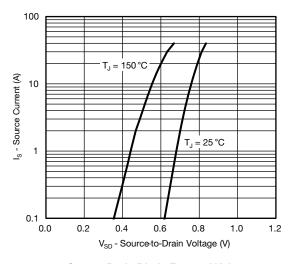
On-Resistance vs. Junction Temperature



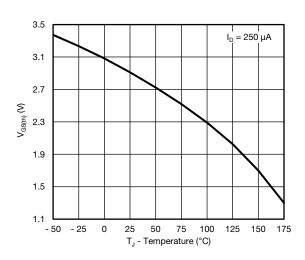
On-Resistance vs. Gate-to-Source Voltage



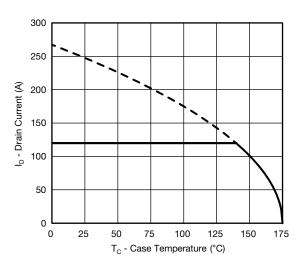
Drain Source Breakdown vs. Junction Temperature



**Source Drain Diode Forward Voltage** 



Threshold Voltage

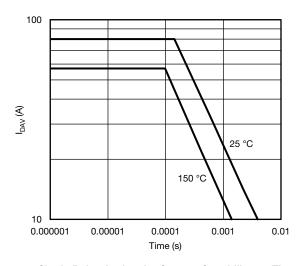


**Current De-rating** 



10 µs

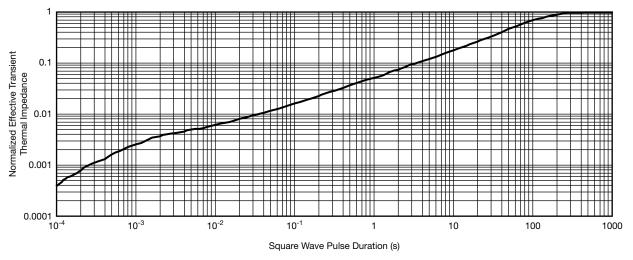
## **THERMAL RATINGS** ( $T_A = 25$ °C, unless otherwise noted)



100 I<sub>D</sub> - Drain Current (A) 100 μs 10 Limited by Bsid 1 1 ms 0.1  $T_C = 25^{\circ}C$ 10 ms Single Pulse **BVDSS** Limited 0.01  $\begin{array}{c} 1 & 10 \\ V_{DS}\text{-} Drain-to-Source Voltage (V) \\ ^*V_{GS}> minimum \ V_{GS} \ at \ which \ R_{DS(on)} \ is \ specified \end{array}$ 0.1 100

Single Pulse Avalanche Current Capability vs. Time





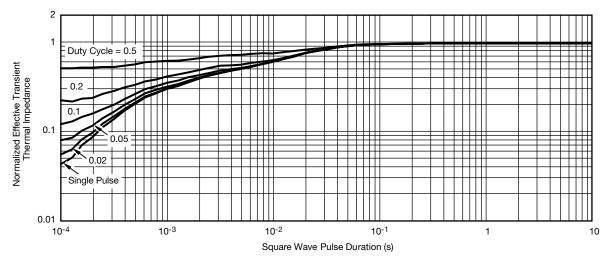
1000

I<sub>DM</sub> Limited

Normalized Thermal Transient Impedance, Junction-to-Ambient



## **THERMAL RATINGS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



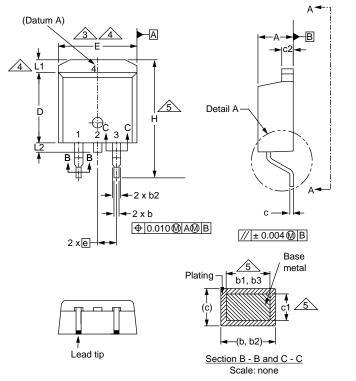
#### Normalized Thermal Transient Impedance, Junction-to-Case

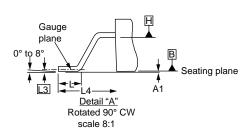
#### Note

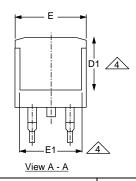
- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction to Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction to Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.



#### **TO-263AB**







	MILLIMETERS			HES
DIM.	MIN.	MAX.	MIN.	MAX.
Α	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
С	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

	MILLIMETERS		INC	HES
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
Е	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
е	2.54 BSC		0.100 BSC	
Н	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010	BSC
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08

DWG: 5970

### Notes

- 1. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 2. Dimensions are shown in millimeters (inches).
- 3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
- 4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
- 5. Dimension b1 and c1 apply to base metal only.
- 6. Datum A and B to be determined at datum plane H.
- 7. Outline conforms to JEDEC outline to TO-263AB.

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