

# BUK962R8-60E-VB Datasheet N-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	60			
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 V$	0.0028			
$R_{DS(on)}(\Omega)$ at $V_{GS} = 4.5 V$	0.0120			
I <sub>D</sub> (A)	210			
Configuration	Single			

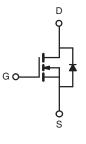
## FEATURES

- Halogen-free According to IEC 61249-2-21
  Definition
- Trench Power MOSFET
- Package with Low Thermal Resistance
- 100 %  $\rm R_g$  and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



HALOGEN





N-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATINGS</b> ( $T_c = 25 \text{ °C}$ , unless otherwise noted)						
PARAMETER		SYMBOL	LIMIT	UNIT		
Drain-Source Voltage		V <sub>DS</sub>	60	M		
Gate-Source Voltage		V <sub>GS</sub>	± 20	V		
Continuous Drain Current	T <sub>C</sub> = 25 °C		210			
	T <sub>C</sub> = 125 °C	I <sub>D</sub>	120 <sup>a</sup>			
Continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	120 <sup>a</sup>	А		
Pulsed Drain Current <sup>b</sup>		I <sub>DM</sub>	480			
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	75			
Single Pulse Avalanche Energy	L = 0.1 MH	E <sub>AS</sub>	281	mJ		
Maximum Power Dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	P	375	W		
	T <sub>C</sub> = 125 °C	P <sub>D</sub>	125	vv		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 175	°C		

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-Ambient	PCB Mount <sup>c</sup>	R <sub>thJA</sub>	40	°C/W	
unction-to-Case (Drain)		R <sub>thJC</sub>	0.4	C/W	

#### Notes

- a. Package limited.
- b. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%.$
- c. When mounted on 1" square PCB (FR-4 material).
- d. Parametric verification ongoing.

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static							<b>I</b>	
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0, I_D = 250 \ \mu A$		60	-	-	v	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$			4.0		
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$		-	-	± 100	nA	
Zero Gate Voltage Drain Current		$V_{GS} = 0 V$	V <sub>DS</sub> = 60 V	-	-	1.0		
	I <sub>DSS</sub>	$V_{GS} = 0 V$	$V_{DS} = 60 \text{ V}, \text{ T}_{J} = 125 ^{\circ}\text{C}$	-	-	50	μA	
		$V_{GS} = 0 V$	V <sub>DS</sub> = 60 V, T <sub>J</sub> = 175 °C	-	-	350		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	$V_{DS} \ge 5 V$	120	-	-	Α	
Drain-Source On-State Resistance <sup>a</sup>		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 30 A	-	0.0028	-	Ω	
	Б	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 30 A, T <sub>J</sub> = 125 °C	-	0.0060	-		
	R <sub>DS(on)</sub>	$V_{GS} = 10 V$	I <sub>D</sub> = 30 A, T <sub>J</sub> = 175 °C	-	0.0080	-		
		$V_{GS} = 4.5 V$	I <sub>D</sub> = 20 A	-	0.012	-		
Forward Transconductanceb	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 30 A		-	109	-	S	
Dynamic <sup>b</sup>								
Input Capacitance	C <sub>iss</sub>		V <sub>DS</sub> = 25 V, f = 1 MHz	-	7300	9125	pF	
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		-	935	1170		
Reverse Transfer Capacitance	C <sub>rss</sub>			-	647	810		
Total Gate Charge <sup>c</sup>	Qg		V <sub>DS</sub> = 30 V, I <sub>D</sub> = 110 A	-	184	276	nC	
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V		-	24.7	-		
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			-	50.4	-		
Gate Resistance	Rg	f = 1 MHz		0.5	1.1	1.6	Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			-	19	29		
Rise Time <sup>c</sup>	t <sub>r</sub>	$\label{eq:VDD} \begin{array}{l} V_{DD}=30~\text{V},~\text{R}_{\text{L}}=0.27~\Omega\\ \text{I}_{\text{D}}\cong110~\text{A},~\text{V}_{\text{GEN}}=10~\text{V},~\text{R}_{\text{g}}=2.5~\Omega \end{array}$		-	23	35	- ns	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	83	125		
Fall Time <sup>c</sup>	t <sub>f</sub>			-	35	53		
Source-Drain Diode Ratings and Char	acteristics <sup>b</sup>							
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	480	Α	
Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> = 100 A, V <sub>GS</sub> = 0		-	0.9	1.5	V	

Notes

a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %.

b. Guaranteed by design, not subject to production testing.

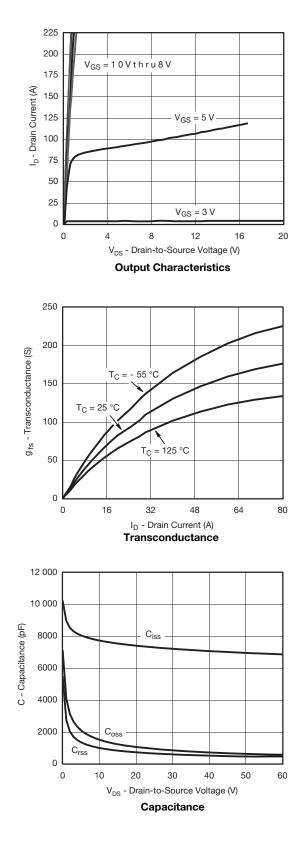
c. Independent of operating temperature.

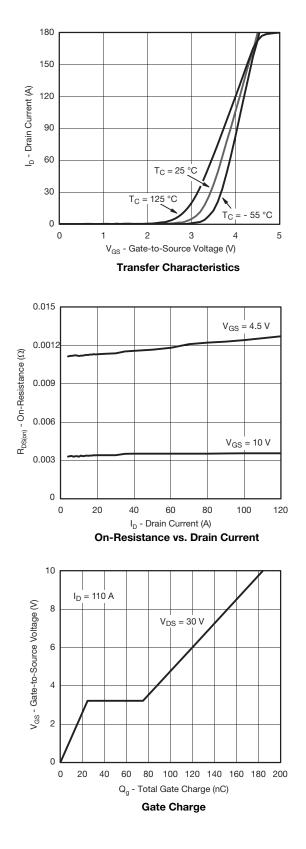
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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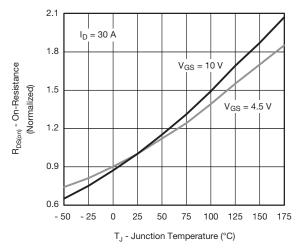
## **TYPICAL CHARACTERISTICS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



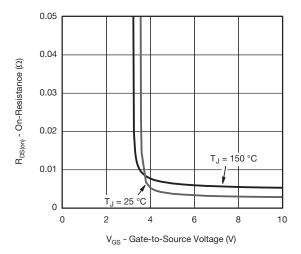




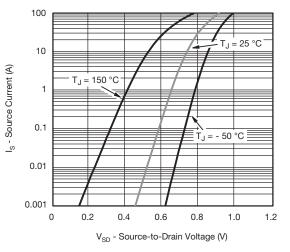
# **TYPICAL CHARACTERISTICS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



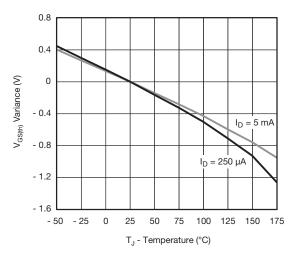




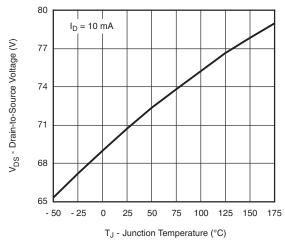
**On-Resistance vs. Gate-to-Source Voltage** 



Source Drain Diode Forward Voltage



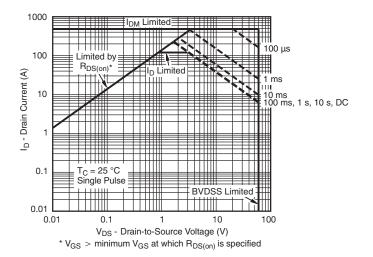




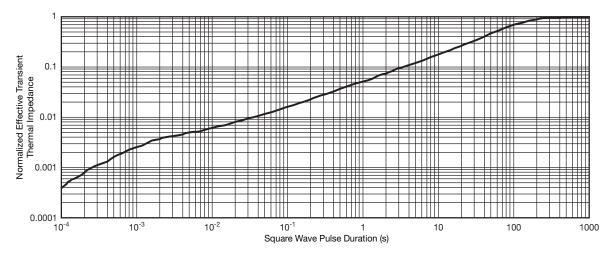
Drain Source Breakdown vs. Junction Temperature



## **THERMAL RATINGS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



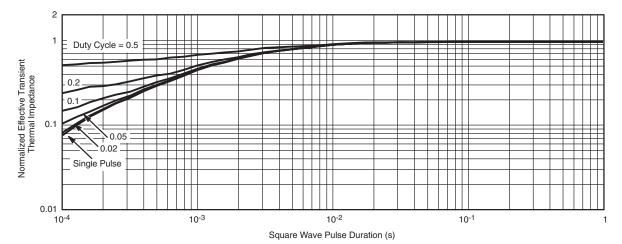
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



## **THERMAL RATINGS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

#### Note

• The characteristics shown in the two graphs

- Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)

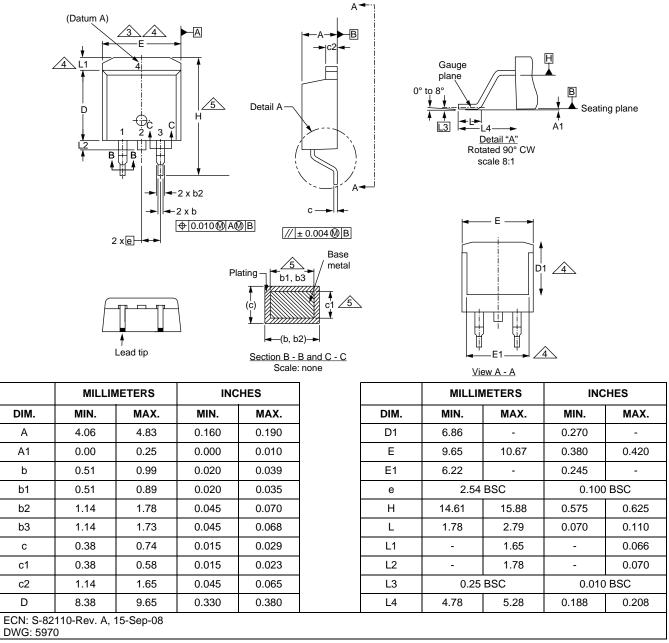
- Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

# BUK962R8-60E-VB



#### **TO-263AB**



#### Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.

2. Dimensions are shown in millimeters (inches).

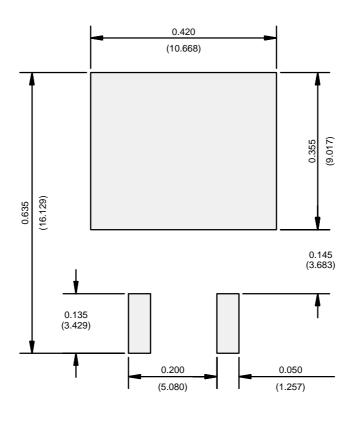
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.

- 4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
- 5. Dimension b1 and c1 apply to base metal only.
- 6. Datum A and B to be determined at datum plane H.

7. Outline conforms to JEDEC outline to TO-263AB.



# **RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads Dimensions in Inches/(mm)



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