

# 60N06L-TQ2-R-VB Datasheet N-Channel 60-V (D-S) MOSFET

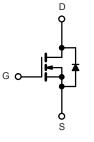
PRODUCT SUMMARY		
V <sub>DS</sub>	60	V
$R_{DS(on)}$ $V_{GS} = 10$ V	11	mΩ
$R_{DS(on)}$ $V_{GS} = 4.5$ V	12	mΩ
I <sub>D</sub>	75	А
Configuration	Sin	gle

#### FEATURES

- 175 °C Junction Temperature
- Trench Power MOSFET







N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> =	25 °C, unless othe	rwise noted)			
Parameter	Symbol	Limit	Unit		
Gate-Source Voltage	V <sub>GS</sub>	± 20	V		
Continuous Drain Current (T 175 °C)	T <sub>C</sub> = 25 °C		75		
Continuous Drain Current (T <sub>J</sub> = 175 °C) <sup>b</sup>	T <sub>C</sub> = 100 °C	D ID	50 <sup>a</sup>		
Pulsed Drain Current	I <sub>DM</sub>	200	Α		
Continuous Source Current (Diode Conduction)	۱ <sub>S</sub>	50 <sup>a</sup>			
Avalanche Current	I <sub>AS</sub>	50	1		
Single Avalanche Energy (Duty Cycle $\leq$ 1 %) L = 0.1 mH		E <sub>AS</sub>	125	mJ	
	T <sub>C</sub> = 25 °C	р	136	14/	
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	3 <sup>b</sup> , 8.3 <sup>b, c</sup>	W	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175	°C		

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	Typical	Maximum	Unit			
Maximum lunction to Ambienta	$t \le 10 \text{ sec}$	P	15	18			
Maximum Junction-to-Ambient <sup>a</sup>	Steady State	R <sub>thJA</sub>	40	50	°C/W		
Maximum Junction-to-Case		R <sub>thJC</sub>	0.85	1.1			
Notes:							

a. Package limited.

b. Surface mounted on 1" x 1" FR4 board.

c.  $t \leq$  10 s.

## 60N06L-TQ2-R-VB



Parameter	Symbol	Test Conditions	Min.	Typ. <sup>a</sup>	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS}$ = 0 V, I <sub>D</sub> = 250 µA	60			V	
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	1		3	v	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS}$ = 0 V, $V_{GS}$ = ± 20 V			± 100	nA	
		$V_{DS}$ = 60 V, $V_{GS}$ = 0 V			1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS}$ = 60 V, $V_{GS}$ = 0 V, $T_{J}$ = 125 °C			50	50 µA	
		$V_{DS}$ = 60 V, $V_{GS}$ = 0 V, $T_{J}$ = 175 °C			250		
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	60			Α	
Drain-Source On-State Resistance <sup>b</sup>		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		0.011			
	Б	$V_{GS}$ = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 125 °C		0.016		Ω	
	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 175 °C		0.020			
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 15 A		0.012			
Forward Transconductance <sup>b</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A		60		S	
Dynamic							
Input Capacitance	C <sub>iss</sub>			4300			
Output Capacitance	C <sub>oss</sub>	$V_{GS}$ = 0 V, $V_{DS}$ = 25 V, f = 1 MHz		470		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>			225		1	
Total Gate Charge <sup>c</sup>	Qg			47		nC	
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	$V_{\rm DS}$ = 30 V, $V_{\rm GS}$ = 10 V, $I_{\rm D}$ = 50 A		10			
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			12		1	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			10	20		
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD}$ = 30 V, $R_L$ = 0.6 $\Omega$		15	25		
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	$\text{I}_\text{D} \cong$ 50 A, $\text{V}_\text{GEN}$ = 10 V, Rg = 2.5 $\Omega$		35	50	ns	
Fall Time <sup>c</sup>	t <sub>f</sub>			20	30		
Source-Drain Diode Ratings and Cha	racteristics (	T <sub>C</sub> = 25 °C)		·	I		
Pulsed Current	I <sub>SM</sub>				60	А	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> = 20 A, V <sub>GS</sub> = 0 V		1	1.5	V	
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 20 A, di/dt = 100 A/μs		45	100	ns	

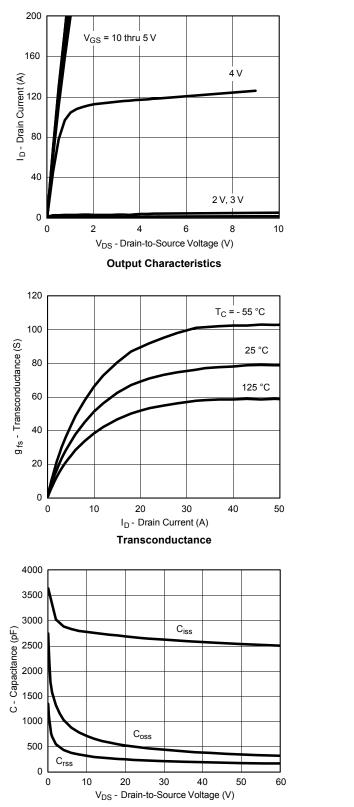
Notes:

a. For design aid only; not subject to production testing. b. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %.

c. Independent of operating temperature.

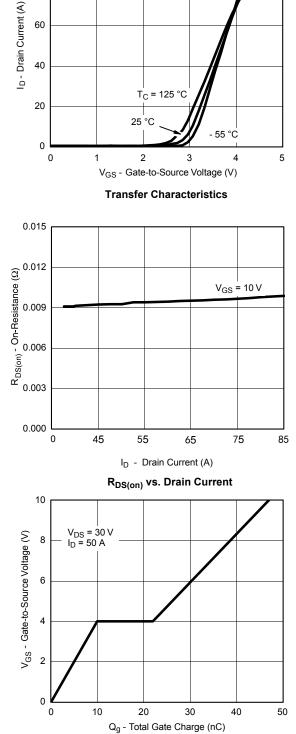
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.





Capacitance

#### TYPICAL CHARACTERISTICS (25 °C unless noted)



**Gate Charge** 

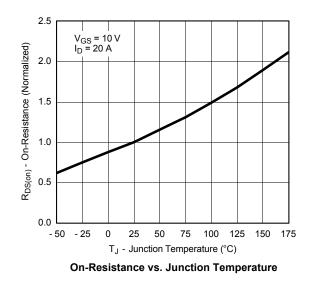
100

80

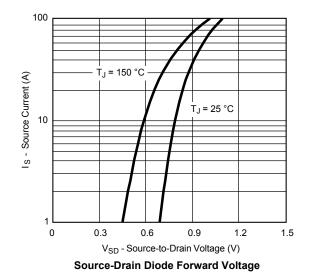
60



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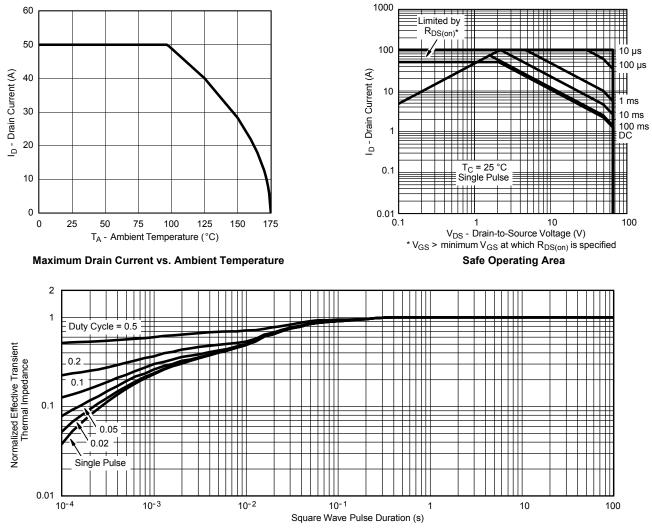


Bsemi

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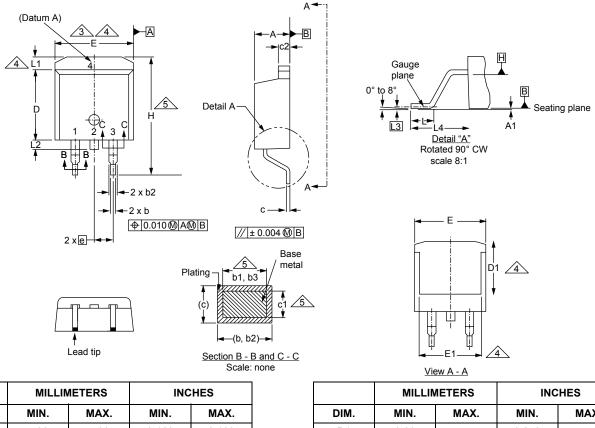
#### THERMAL RATINGS



Normalized Thermal Transient Impedance, Junction-to-Case



#### **TO-263AB (HIGH VOLTAGE)**



DIM.	MILLIMETERS		INCHES			MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.	DIM.	MIN.	MAX.	MIN.	M		
А	4.06	4.83	0.160	0.190	D1	6.86	-	0.270			
A1	0.00	0.25	0.000	0.010	E	9.65	10.67	0.380	0.		
b	0.51	0.99	0.020	0.039	E1	6.22	-	0.245			
b1	0.51	0.89	0.020	0.035	е	2.54 BSC		e 2.54 BSC		0.100	BSC
b2	1.14	1.78	0.045	0.070	Н	14.61	15.88	0.575	0.0		
b3	1.14	1.73	0.045	0.068	L	1.78	2.79	0.070	0.		
с	0.38	0.74	0.015	0.029	L1	-	1.65	-	0.0		
c1	0.38	0.58	0.015	0.023	L2	-	1.78	-	0.0		
c2	1.14	1.65	0.045	5 0.065		0.25 BSC		0.010	BSC		
D	8.38	9.65	0.330	0.380	L4	4.78	5.28	0.188	0.2		

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.

2. Dimensions are shown in millimeters (inches).

Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.

4. Thermal PAD contour optional within dimension E, L1, D1 and E1.

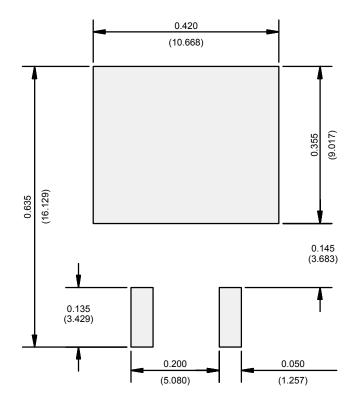
5. Dimension b1 and c1 apply to base metal only.

6. Datum A and B to be determined at datum plane H.

7. Outline conforms to JEDEC outline to TO-263AB.



#### **RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads Dimensions in Inches/(mm)



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