

## STH270N4F3-6-VB Datasheet N-Channel 40 V (D-S) 175 °C MOSFET

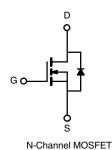
PRODUCT SUMMARY					
V <sub>DS</sub> (V)	40				
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.0015				
I <sub>D</sub> (A)	200				
Configuration	Single				
Package	TO-263-7L				

#### **FEATURES**

- Trench power MOSFET
- Package with low thermal resistance
- $\bullet$  100 %  $R_g$  and UIS tested







ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	LIMIT	UNIT			
Drain-Source Voltage		$V_{DS}$	40	V		
Gate-Source Voltage		$V_{GS}$	± 20	V		
Continuous Drain Current	$T_C = 25  ^{\circ}C$ a	I-	200			
Continuous Drain Current	T <sub>C</sub> = 125 °C	l <sub>D</sub>	192			
Continuous Source Current (Diode Conduction) a	I <sub>S</sub>	200	Α			
Pulsed Drain Current <sup>b</sup>	I <sub>DM</sub>	600				
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	85			
Single Pulse Avalanche Energy	L = 0.1 IIII1	E <sub>AS</sub>	361	mJ		
Maximum Power Dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	P <sub>D</sub>	375	W		
	T <sub>C</sub> = 125 °C	ıр	125	VV		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C		

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	LIMIT	UNIT		
Junction-to-Ambient	PCB Mount <sup>c</sup>	$R_{thJA}$	40	°C/W		
Junction-to-Case (Drain)		R <sub>thJC</sub>	0.4	G/ VV		

#### Notes

- a. Package limited.
- b. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.
- c. When mounted on 1" square PCB (FR4 material).
- d. Parametric verification ongoing.

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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		40	-	-	V
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$		3.0	3.5	V
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 40 V	-	-	1	μА
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 125 °C	=	-	50	
		$V_{GS} = 0 V$	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 175 °C	-	-	250	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	$V_{DS} \ge 5 \text{ V}$	200	-	-	Α
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 30 A	=	0.0015	-	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 30 A, T <sub>J</sub> = 125 °C	-	0.0028	-	Ω
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 30 A, T <sub>J</sub> = 175 °C	-	0.0034	-	
Forward Transconductance b	9 <sub>fs</sub>	V <sub>DS</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 30 A		198	-	S
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>			1	13 880	17 350	
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$	-	1414	1770	pF
Reverse Transfer Capacitance	C <sub>rss</sub>			1	840	1050	
Total Gate Charge <sup>c</sup>	Qg			-	206	310	
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	$V_{GS} = 10 \text{ V}$	$V_{DS} = 20 \text{ V}, I_{D} = 120 \text{ A}$	-	50	-	nC
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			-	44	-	
Gate Resistance	$R_g$	f = 1 MHz		0.25	8.0	1.8	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>				26	39	
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD}$ = 20 V, $R_L$ = 0.17 $\Omega$ $I_D$ $\cong$ 120 A, $V_{GEN}$ = 10 V, $R_g$ = 1 $\Omega$		-	21	32	ns
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	68	102	
Fall Time <sup>c</sup>	t <sub>f</sub>			-	12	18	
Source-Drain Diode Ratings and Characteristics <sup>b</sup>							
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	600	Α
Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> = 80 A, V <sub>GS</sub> = 0 V		-	0.86	1.5	V

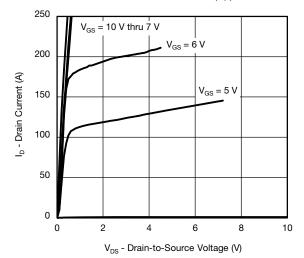
#### Notes

- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

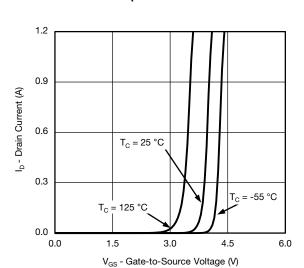
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



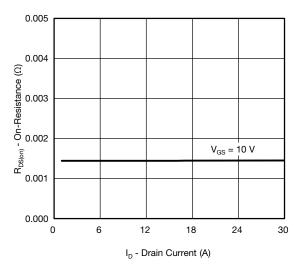
### **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



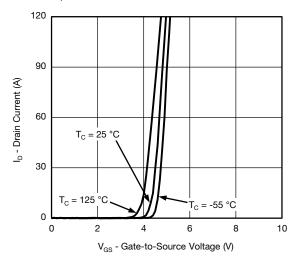




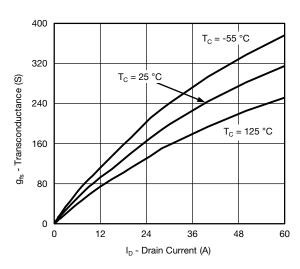
Transfer Characteristics



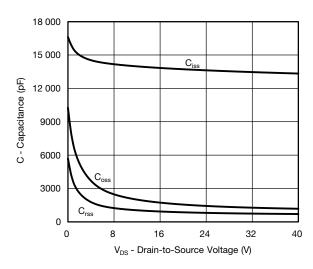
On-Resistance vs. Drain Current



**Transfer Characteristics** 



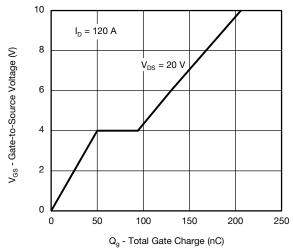
Transconductance



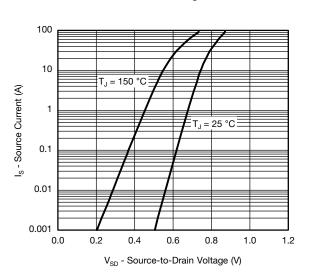
Capacitance



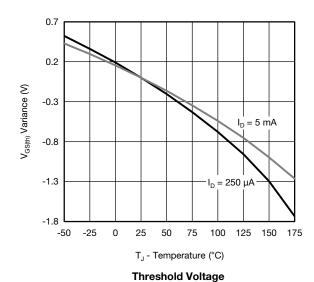
## **TYPICAL CHARACTERISTICS** ( $T_A = 25$ °C, unless otherwise noted)



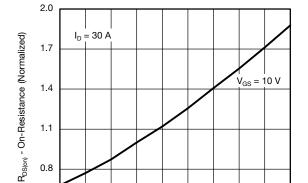




**Source Drain Diode Forward Voltage** 



4



0.5

-50

-25 0 25

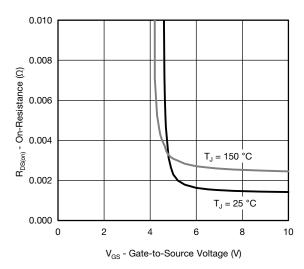
T<sub>J</sub> - Junction Temperature (°C)

50

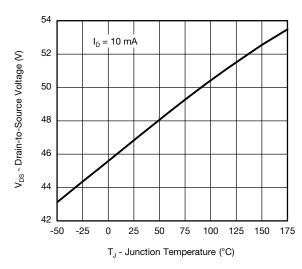
75

100 125

#### On-Resistance vs. Junction Temperature



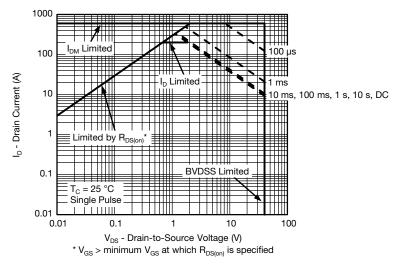
On-Resistance vs. Gate-to-Source Voltage



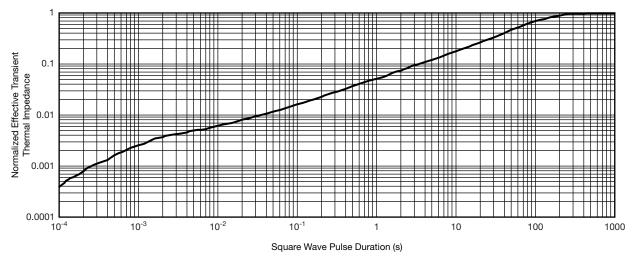
Drain Source Breakdown vs. Junction Temperature



### **THERMAL RATINGS** ( $T_A = 25$ °C, unless otherwise noted)



#### Safe Operating Area

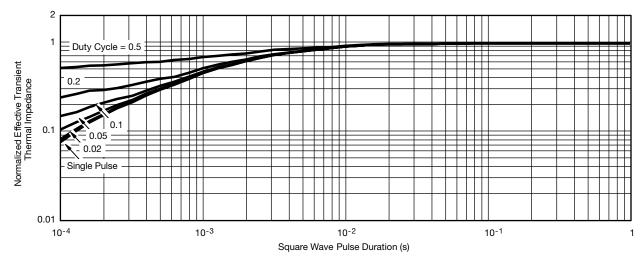


Normalized Thermal Transient Impedance, Junction-to-Ambient

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### **THERMAL RATINGS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



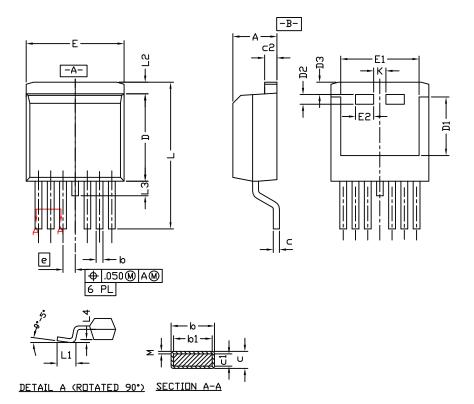
Normalized Thermal Transient Impedance, Junction-to-Case

#### Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.



# D<sup>2</sup>PAK (TO-263-7L) Case Outline



#### **Notes**

- 1. Plane B includes maximum features of heat sink tab and plastic.
- 2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- 3. Pin to pin coplanarity max. 4 mils.
- 4. Lead thickness 25 mils.
- 5. For SUM part numbers lead thickness is 24 mils to 29 mils.
- 6. For reference only.
- 7. Use inches as the primary measurement.
- 8. This feature is only for SUM.

	INCHES		MILLIN	METERS	
DIM.	MIN.	MAX.	MIN.	MAX.	
Α	0.160	0.190	4.064	4.826	
b	0.020	0.039	0.508	0.990	
b1	0.020	0.035	0.508	0.889	
b2	0.045	0.055	1.143	1.397	
c* SUB	0.012	0.018	0.305	0.457	
c* SUM	0.022	0.028	0.559	0.711	
c1	0.018	0.025	0.457	0.635	
c2	0.045	0.055	1.143	1.397	
D	0.340	0.380	8.636	9.652	
D1	0.220	0.240	5.588	6.096	
D2	0.038	0.042	0.965	1.067	
D3	0.045	0.055	1.143	1.397	
Е	0.380	0.410	9.652	10.414	
E1	0.245	-	6.223	-	
E2	0.072	0.078	1.829	1.981	
е	0.050	BSC	1.27 BSC		
K	0.045	0.055	1.143	1.397	
L	0.575	0.625	14.605	15.875	
L1	0.090	0.110	2.286	2.794	
L2	0.040	0.055	1.016	1.397	
L3	0.050	0.070	1.270	1.778	
L4	0.010 BSC		0.254 BSC		
М	п	0.002 -		0.050	
ECN: T13-0709-Rev. B, 30-Sep-13					

DWG: 6006



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