

## SiHFBF20L-E3-VB Datasheet

### Power MOSFET

#### PRODUCT SUMMARY

$V_{DS}$ (V)	950	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	5.4
$Q_g$ (Max.) (nC)	78	
$Q_{gs}$ (nC)	10	
$Q_{gd}$ (nC)	42	
Configuration	Single	

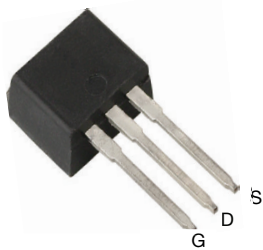
#### FEATURES

- Dynamic  $dV/dt$  Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC

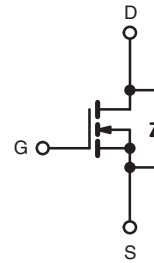


Available  
**RoHS\***  
 COMPLIANT

TO-262



Top View



N-Channel MOSFET

#### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

PARAMETER			SYMBOL	LIMITE	UNIT
Drain-Source Voltage			$V_{DS}$	950	V
Gate-Source Voltage			$V_{GS}$	$\pm 20$	
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25\text{ }^{\circ}\text{C}$	$I_D$	3.6	A
		$T_C = 100\text{ }^{\circ}\text{C}$		2.3	
Pulsed Drain Current <sup>a</sup>			$I_{DM}$	14	
Linear Derating Factor				1.0	W/ $^{\circ}\text{C}$
Single Pulse Avalanche Energy <sup>b</sup>			$E_{AS}$	250	mJ
Repetitive Avalanche Current <sup>a</sup>			$I_{AR}$	3.6	A
Repetitive Avalanche Energy <sup>a</sup>			$E_{AR}$	13	mJ
Maximum Power Dissipation	$T_C = 25\text{ }^{\circ}\text{C}$		$P_D$	125	W
Peak Diode Recovery $dV/dt^c$			$dV/dt$	1.5	V/ns
Operating Junction and Storage Temperature Range			$T_J, T_{stg}$	- 55 to + 150	$^{\circ}\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s			300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 36\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 3.6\text{ A}$  (see fig. 12).
- $I_{SD} \leq 3.6\text{ A}$ ,  $dI/dt \leq 70\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq 600$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.50	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.0	

**SPECIFICATIONS** ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		950	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	1.1	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 900 V, V <sub>GS</sub> = 0 V		-	-	100	μA
		V <sub>DS</sub> = 720 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	500	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 2.2 A <sup>b</sup>	—	5.4	-	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 100 V, I <sub>D</sub> = 2.2 A <sup>b</sup>		2.3	-	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5		-	1200	-	pF
Output Capacitance	C <sub>oss</sub>			-	320	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	200	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 3.6 A, V <sub>DS</sub> = 360 V, see fig. 6 and 13 <sup>b</sup>	-	-	78	nC
Gate-Source Charge	Q <sub>gs</sub>			-	-	10	
Gate-Drain Charge	Q <sub>gd</sub>			-	-	42	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 450 V, I <sub>D</sub> = 3.6 A, R <sub>g</sub> = 12 Ω, R <sub>D</sub> = 120 Ω, see fig. 10 <sup>b</sup>		-	14	-	ns
Rise Time	t <sub>r</sub>			-	25	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	90	-	
Fall Time	t <sub>f</sub>			-	30	-	
Internal Drain Inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	L <sub>S</sub>			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	3.6	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	14	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 3.6 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	1.8	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 3.6 A, dI/dt = 100 A/μs <sup>b</sup>		-	430	650	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	1.4	2.1	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
 b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

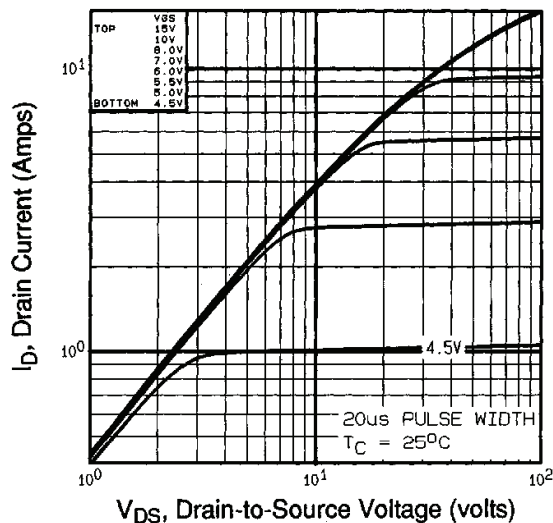


Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^{\circ}\text{C}$

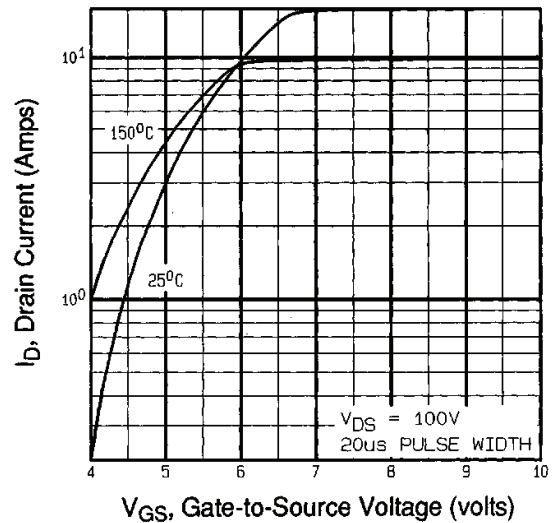


Fig. 3 - Typical Transfer Characteristics

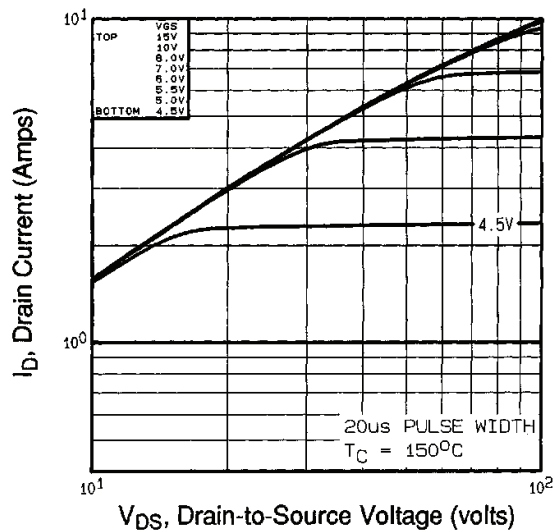


Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^{\circ}\text{C}$

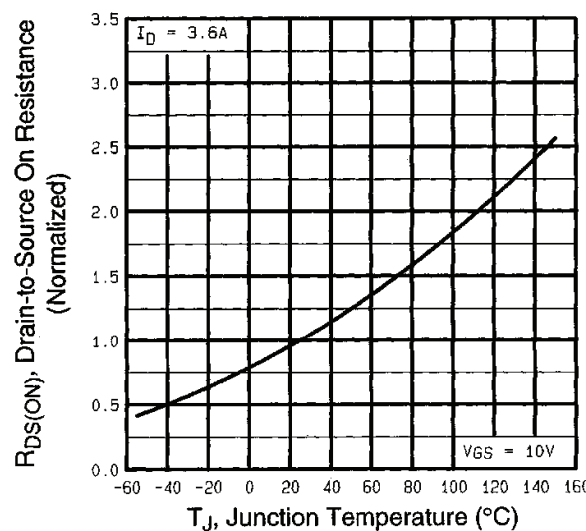


Fig. 4 - Normalized On-Resistance vs. Temperature

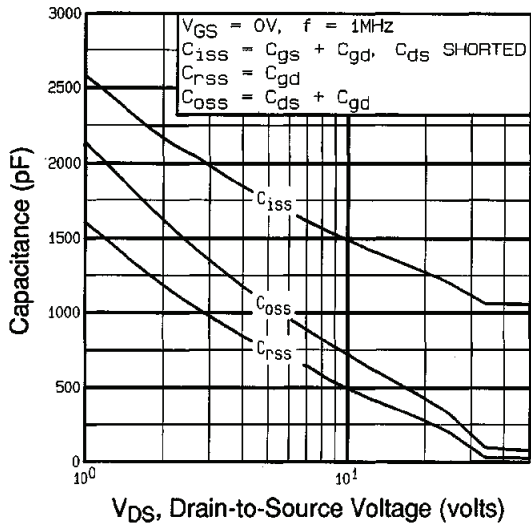


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

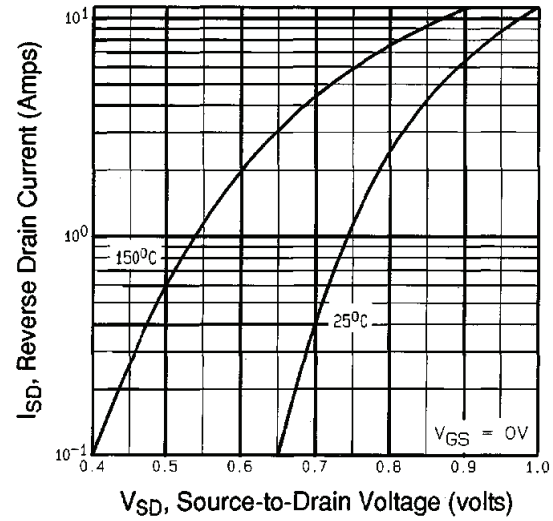


Fig. 7 - Typical Source-Drain Diode Forward Voltage

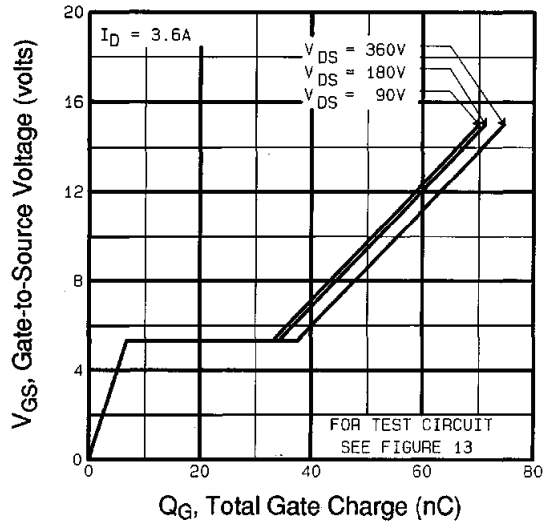


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

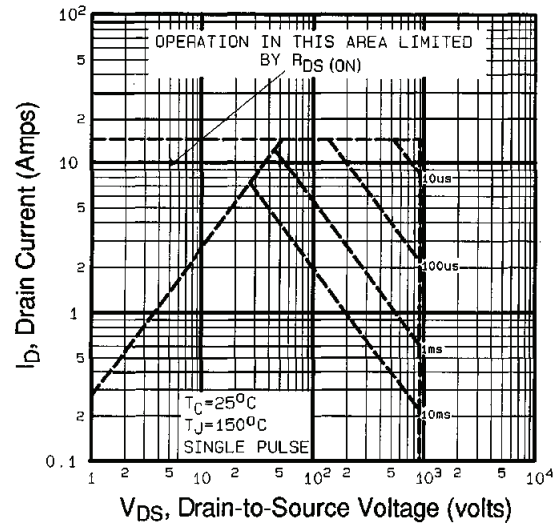


Fig. 8 - Maximum Safe Operating Area

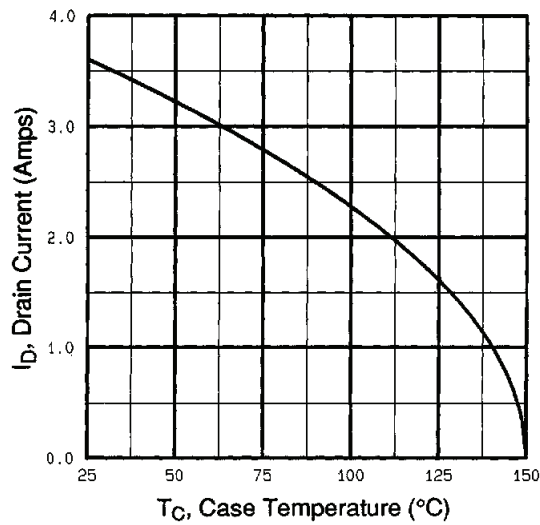


Fig. 9 - Maximum Drain Current vs. Case Temperature

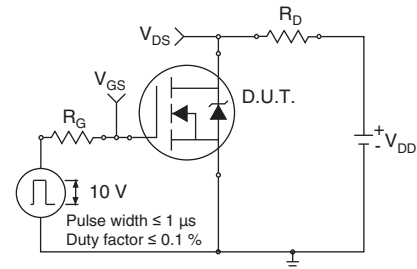


Fig. 10a - Switching Time Test Circuit

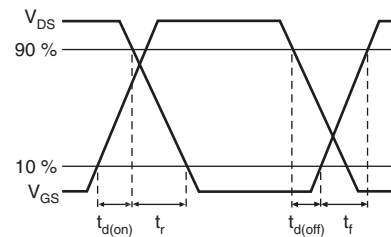


Fig. 10b - Switching Time Waveforms

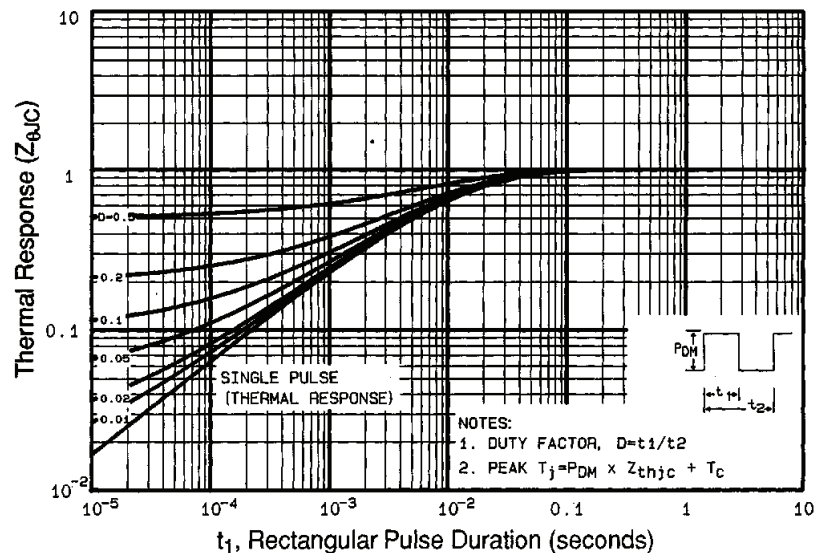


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

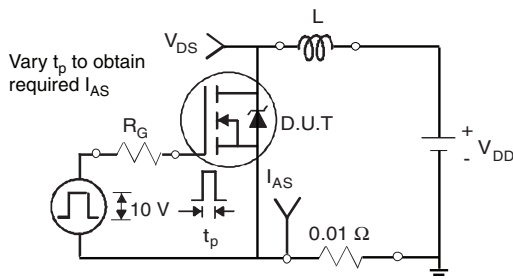


Fig. 12a - Unclamped Inductive Test Circuit

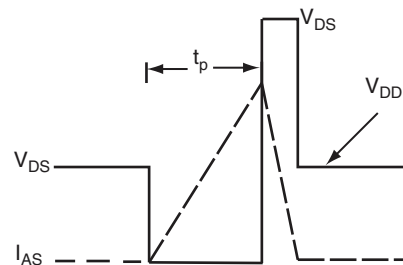


Fig. 12b - Unclamped Inductive Waveforms

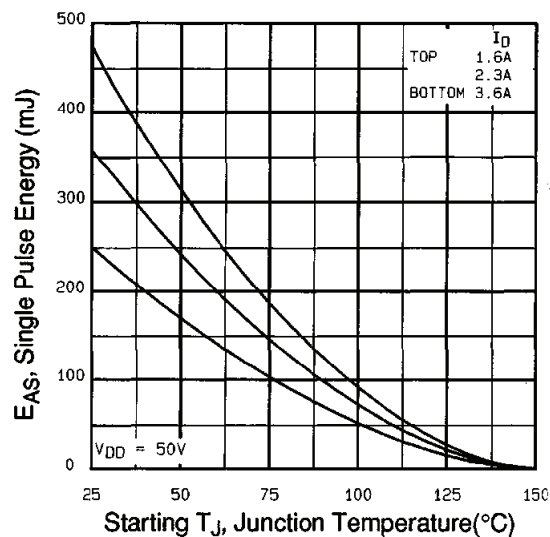


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

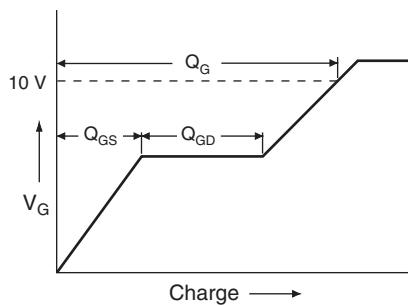


Fig. 13a - Basic Gate Charge Waveform

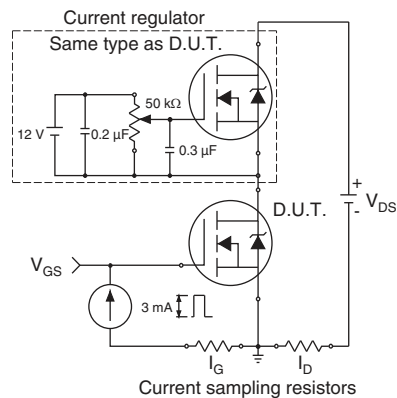
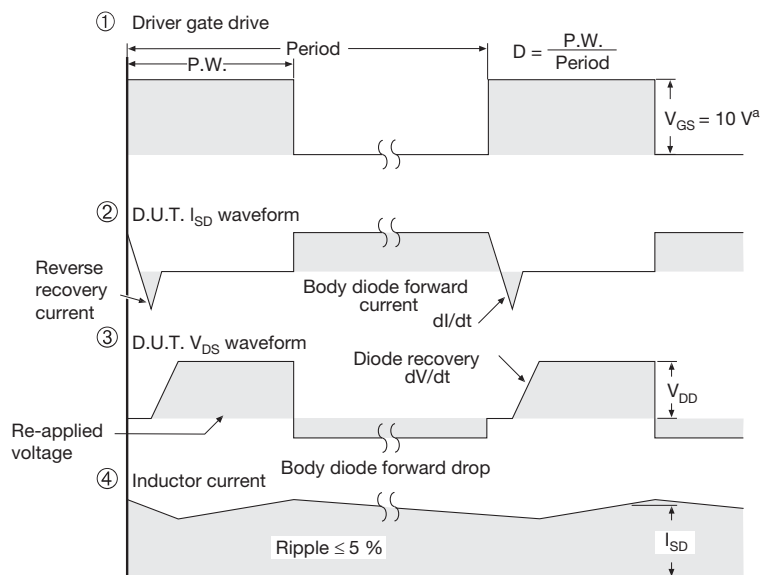
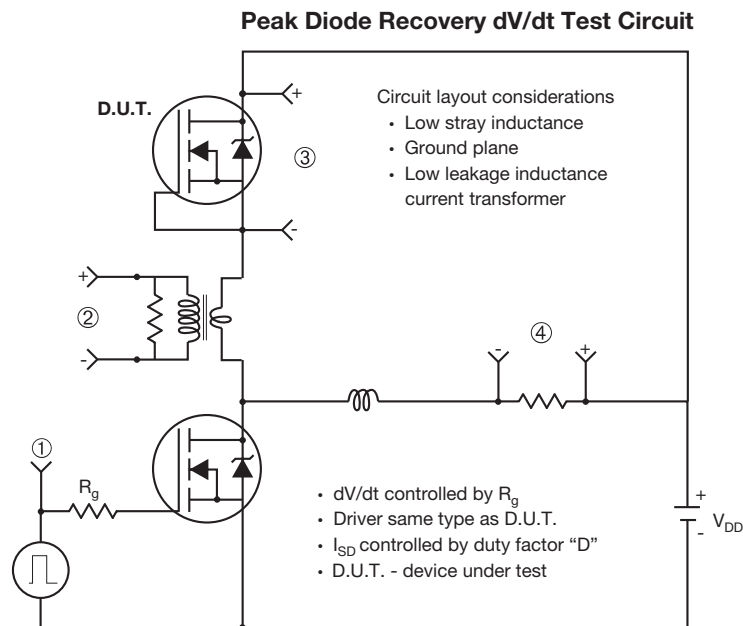
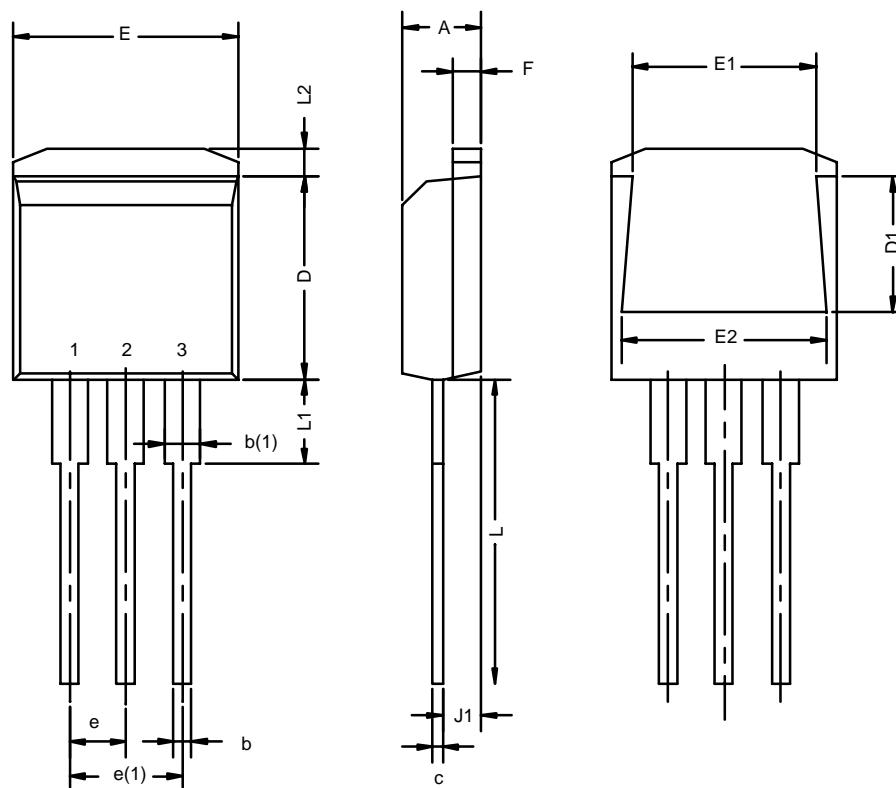


Fig. 13b - Gate Charge Test Circuit

**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

**TO-262: 3-LEAD**

Dim	MILLIMETERS*		INCHES	
	Min	Max	Min	Max
<b>A</b>	4.32	4.70	0.170	0.185
<b>b</b>	0.64	1.00	0.025	0.039
<b>b(1)</b>	1.14	1.40	0.045	0.055
<b>c</b>	0.36	0.50	0.014	0.020
<b>D</b>	8.64	9.65	0.340	0.380
<b>D1</b>	5.59	6.10	0.220	0.240
<b>e</b>	2.41	2.67	0.095	0.105
<b>e(1)</b>	4.95	5.33	0.195	0.210
<b>E</b>	10.03	10.41	0.395	0.410
<b>E1</b>	7.87	8.64	0.310	0.340
<b>E2</b>	9.02	9.53	0.355	0.375
<b>F</b>	1.14	1.40	0.045	0.055
<b>J1</b>	2.41	2.79	0.095	0.110
<b>L</b>	13.08	14.22	0.515	0.560
<b>L1</b>	-	3.81	-	0.150
<b>L2</b>	1.02	1.40	0.040	0.055

ECN: T-02234—Rev. C, 14-Oct-02  
 DWG: 5855

\*Use millimeters as the primary measurement



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