

NP48N055NLE-VB Datasheet

Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	60	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.015
Q_g (Max.) (nC)	110	
Q_{gs} (nC)	29	
Q_{gd} (nC)	36	
Configuration	Single	

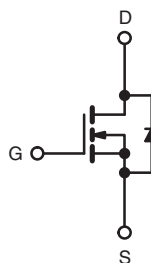
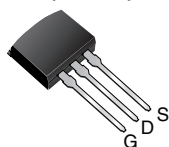
FEATURES

- Advanced process technology
- 175 °C operating temperature
- Fast switching



RoHS*
Available
HALOGEN
FREE
Available

I²PAK (TO-262)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	60	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current ^f	V_{GS} at 10 V	$T_C = 25\text{ }^{\circ}\text{C}$	I_D	60	A
		$T_C = 100\text{ }^{\circ}\text{C}$		50	
Pulsed Drain Current ^{a, e}			I_{DM}	290	
Linear Derating Factor				1.3	W/ $^{\circ}\text{C}$
Single Pulse Avalanche Energy ^{b, e}			E_{AS}	100	mJ
Maximum Power Dissipation	$T_C = 25\text{ }^{\circ}\text{C}$		P_D	190	W
	$T_A = 25\text{ }^{\circ}\text{C}$			3.7	
Peak Diode Recovery dV/dt ^{c, e}			dV/dt	4.5	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to +175	$^{\circ}\text{C}$
Soldering Recommendations (Peak temperature) ^d	for 10 s			300	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25\text{ V}$, Starting $T_J = 25\text{ }^{\circ}\text{C}$, $L = 22\text{ }\mu\text{H}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 72\text{ A}$ (see fig. 12).
- $I_{SP} \leq 72\text{ A}$, $dI/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 175\text{ }^{\circ}\text{C}$.
- 1.6 mm from case.
- Uses IRFZ48, SiHFZ48 data and test conditions.
- Calculated continuous current based on maximum allowable junction temperature.


THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB mount) ^a	R_{thJA}	-	40	°C / W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.8	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

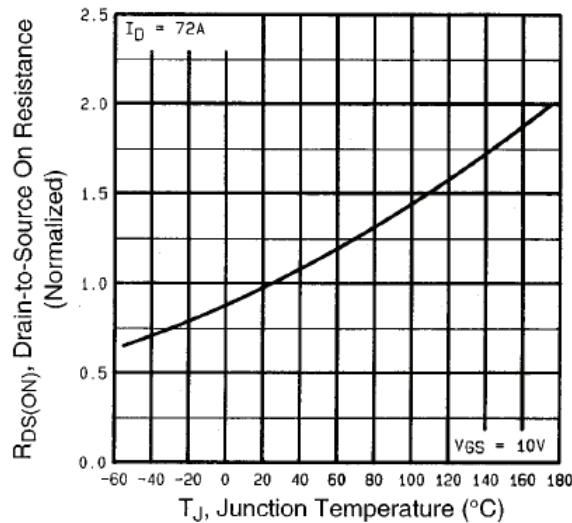
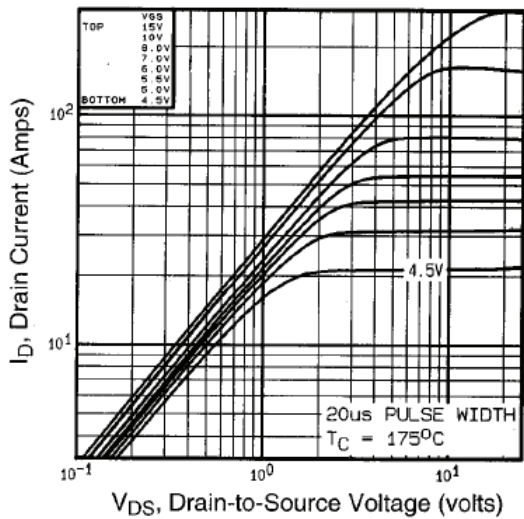
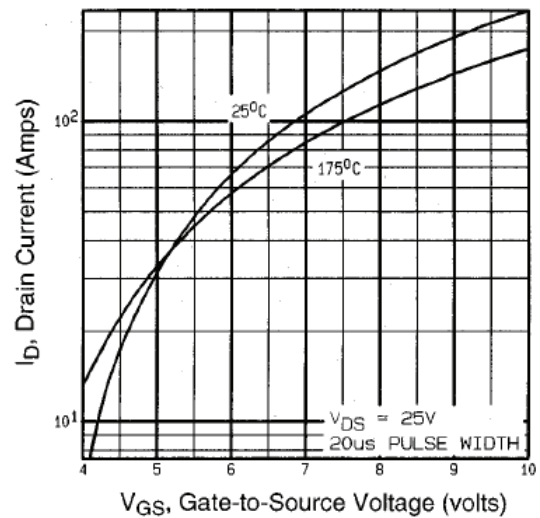
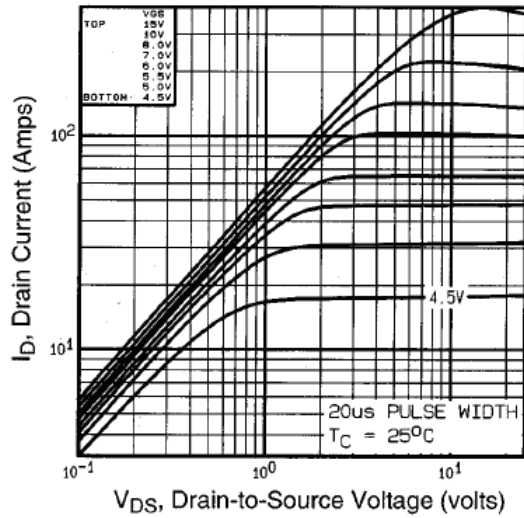
SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$	60	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$, $I_D = 1\text{ mA}$ ^c	-	0.060	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.5	-	3.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	μA
		$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^{\circ}\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$ ^b	-	0.015	-	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 25\text{ V}, I_D = 15\text{ A}$ ^b	27	-	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V},$ $V_{DS} = 25\text{ V},$ $f = 1.0\text{ MHz, see fig. 5 }^c$	-	3500	-	pF
Output Capacitance	C_{oss}		-	1300	-	
Reverse Transfer Capacitance	C_{rss}		-	190	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}, I_D = 12\text{ A}, V_{DS} = 48\text{ V},$ see fig. 6 and 13 ^{b, c}	-	-	110	nC
Gate-Source Charge	Q_{gs}		-	-	29	
Gate-Drain Charge	Q_{gd}		-	-	36	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30\text{ V}, I_D = 12\text{ A},$ $R_g = 9.1\text{ }\Omega, R_D = 0.34\text{ }\Omega,$ see fig. 10 ^{b, c}	-	8.1	-	ns
Rise Time	t_r		-	250	-	
Turn-Off Delay Time	$t_{d(off)}$		-	210	-	
Fall Time	t_f		-	250	-	
Internal Source Inductance	L_S	Between lead, and center of die contact	-	7.5	-	nH
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	50 ^c	A
Pulsed Diode Forward Current ^a	I_{SM}		-	-	90	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^{\circ}\text{C}, I_S = 72\text{ A}, V_{GS} = 0\text{ V}$ ^b	-	-	2.0	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^{\circ}\text{C}, I_F = 72\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}$ ^{b, c}	-	120	180	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	500	800	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
 b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
 c. Uses VBL1615/NP48N055NLE-VB data and test conditions.
 d. Calculated continuous current based on maximum allowable junction temperature.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



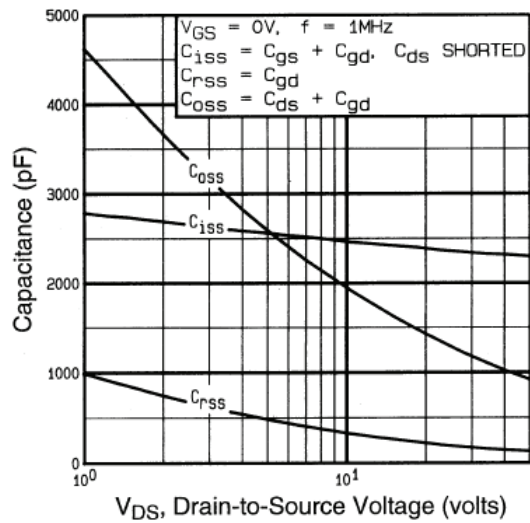


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

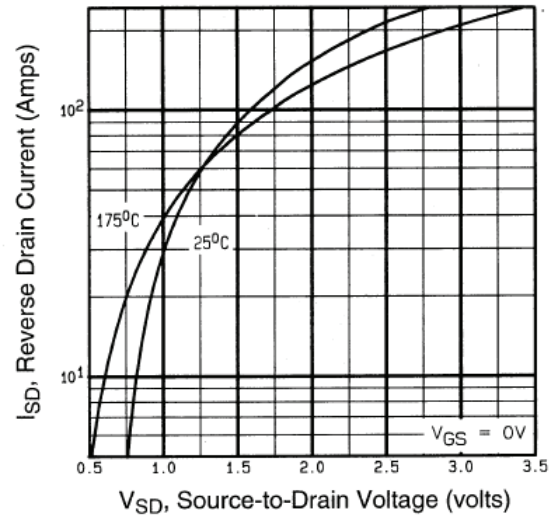


Fig. 7 - Typical Source-Drain Diode Forward Voltage

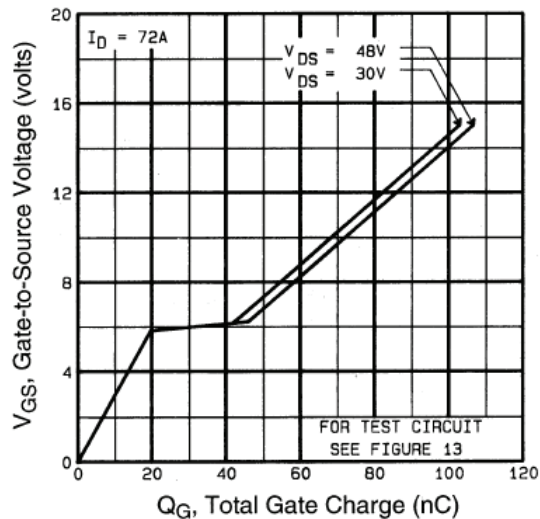


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

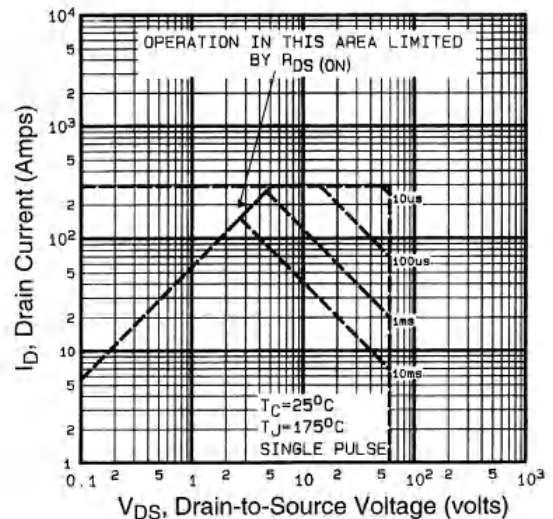


Fig. 8 - Maximum Safe Operating Area

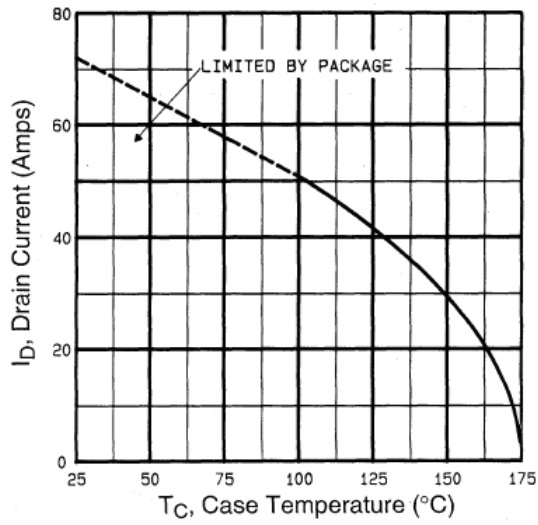


Fig. 9 - Maximum Drain Current vs. Case Temperature

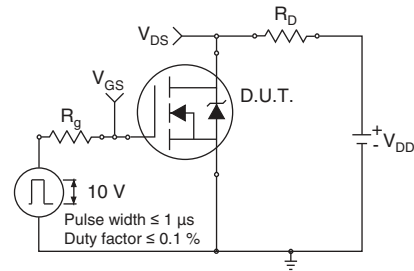


Fig. 10a - Switching Time Test Circuit

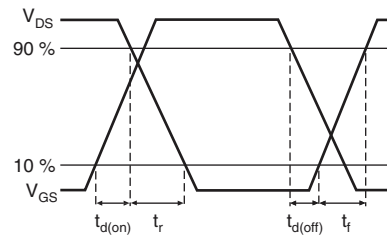


Fig. 10b - Switching Time Waveform

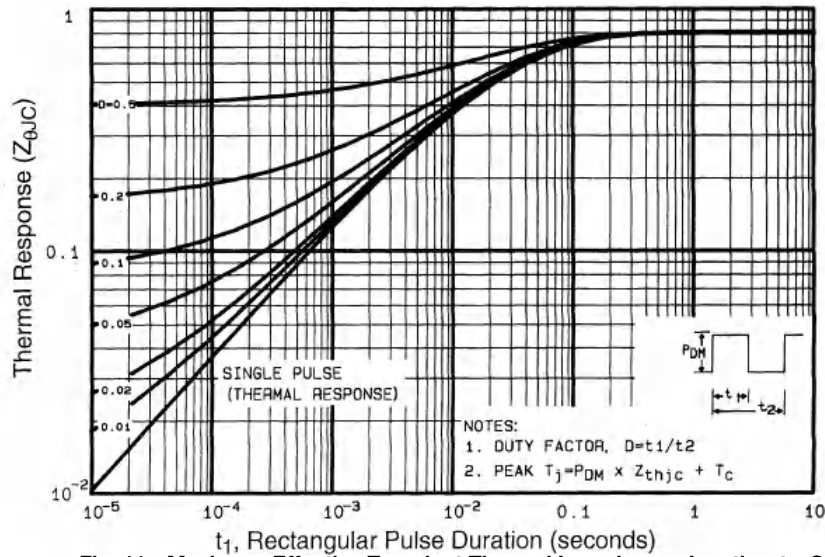


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

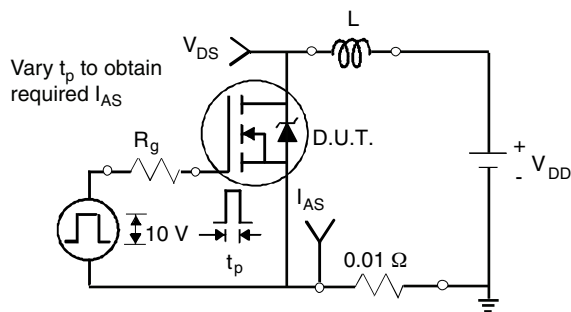


Fig. 12a - Unclamped Inductive Test Circuit

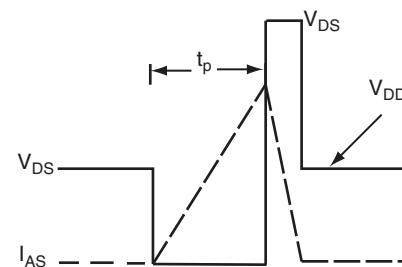


Fig. 12b - Unclamped Inductive Waveforms

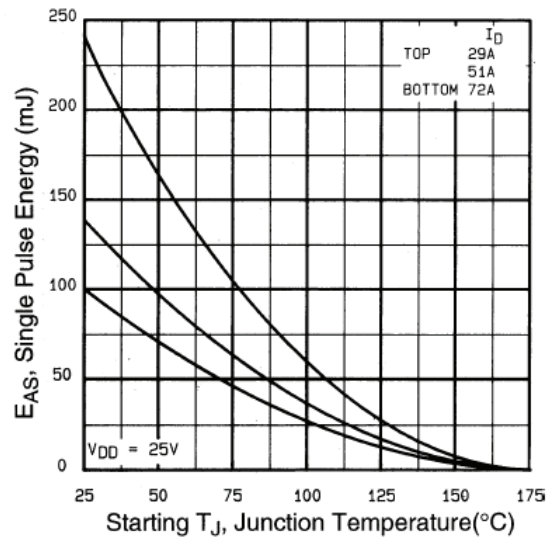


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

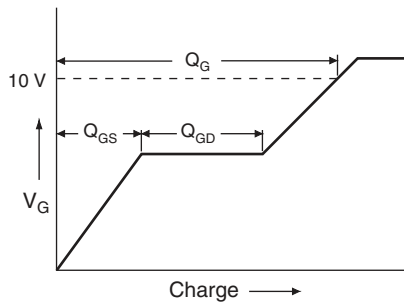


Fig. 13a - Maximum Avalanche Energy vs. Drain Current

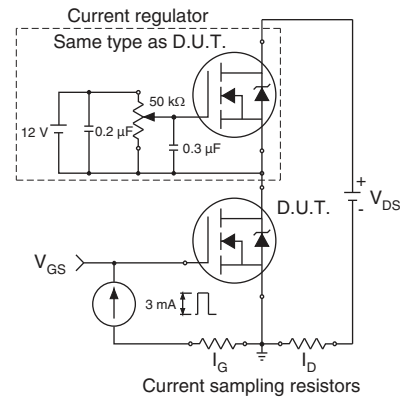
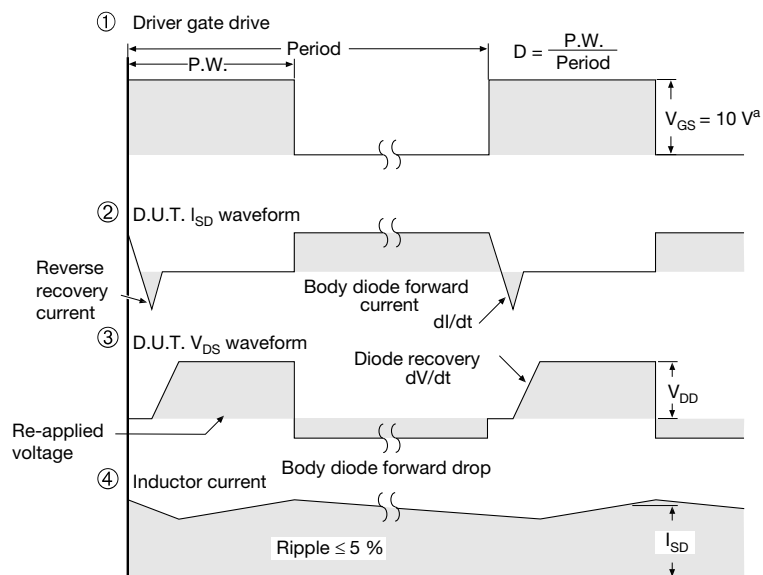
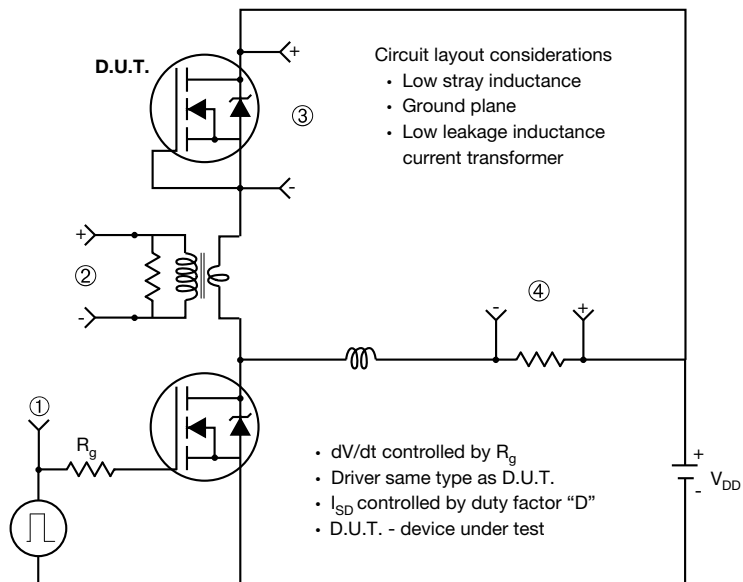
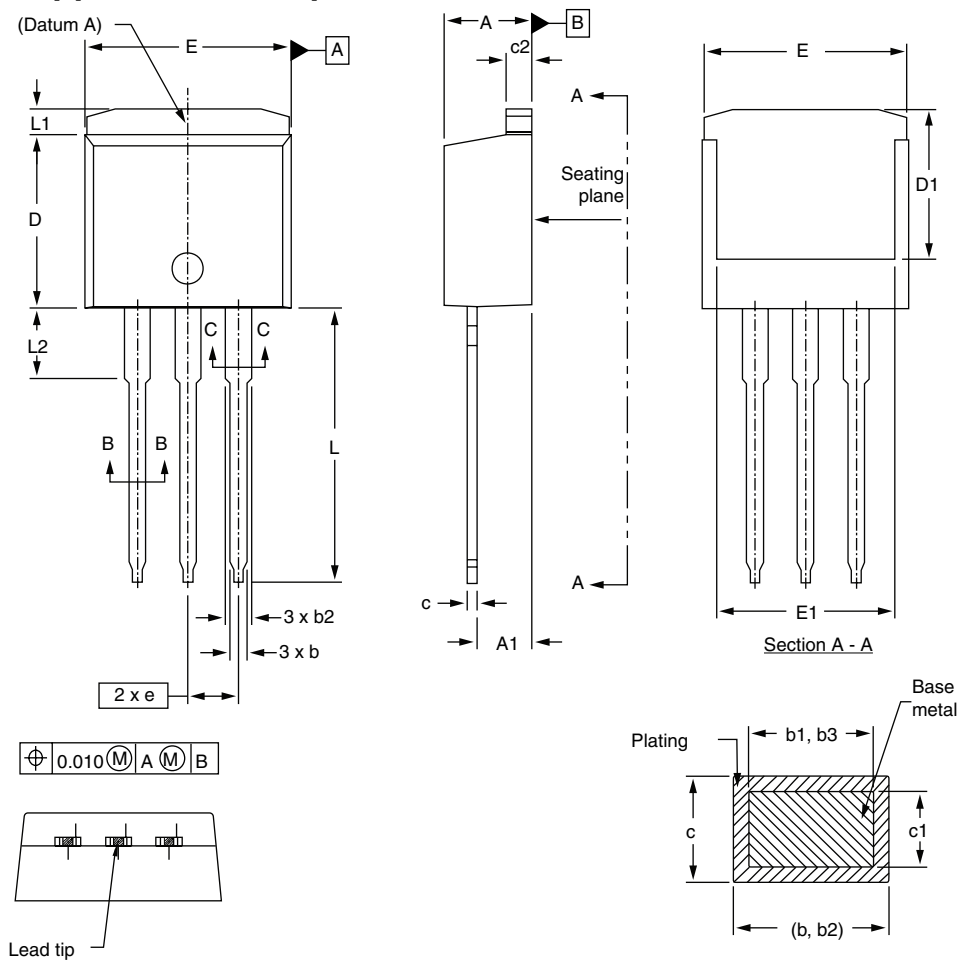


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit**Note**

a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

I²PAK (TO-262) (HIGH VOLTAGE)
 Section B - B and C - C
 Scale: None

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	2.03	3.02	0.080	0.119
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D	8.38	9.65	0.330	0.380
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
L	13.46	14.10	0.530	0.555
L1	-	1.65	-	0.065
L2	3.56	3.71	0.140	0.146

 ECN: S-82442-Rev. A, 27-Oct-08
 DWG: 5977
Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outmost extremes of the plastic body.
3. Thermal pad contour optional within dimension E, L1, D1, and E1.
4. Dimension b1 and c1 apply to base metal only.

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