

## K3821-VB Datasheet

### Power MOSFET

#### PRODUCT SUMMARY

$V_{DS}$ (V)	100	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	0.020
$Q_g$ (Max.) (nC)	70	
$Q_{gs}$ (nC)	13	
$Q_{gd}$ (nC)	39	
Configuration	Single	

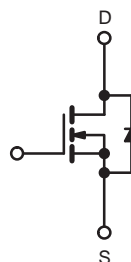
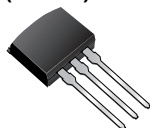
#### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Surface Mount
- Low-Profile Through-Hole
- Available in Tape and Reel
- Dynamic  $dV/dt$  Rating
- 150 °C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Compliant to RoHS Directive 2002/95/EC



**RoHS\***  
COMPLIANT  
HALOGEN  
**FREE**  
Available

I<sup>2</sup>PAK  
(TO-262)



N-Channel MOSFET

#### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

PARAMETER				SYMBOL	LIMIT	UNIT
Drain-Source Voltage				$V_{DS}$	100	V
Gate-Source Voltage				$V_{GS}$	$\pm 20$	
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25\text{ }^{\circ}\text{C}$	$I_D$	50	A	
		$T_C = 100\text{ }^{\circ}\text{C}$		43		
Pulsed Drain Current <sup>a, e</sup>				$I_{DM}$		72
Linear Derating Factor					1.0	W/ $^{\circ}\text{C}$
Single Pulse Avalanche Energy <sup>b, e</sup>				$E_{AS}$	580	mJ
Avalanche Current <sup>a</sup>				$I_{AR}$	20	A
Repetitive Avalanche Energy <sup>a</sup>				$E_{AR}$	13	mJ
Maximum Power Dissipation	$T_C = 25\text{ }^{\circ}\text{C}$			$P_D$	3.1	W
	$T_A = 25\text{ }^{\circ}\text{C}$				130	
Peak Diode Recovery $dV/dt$ <sup>c, e</sup>				$dV/dt$	5.0	V/ns
Operating Junction and Storage Temperature Range				$T_J, T_{stg}$	- 55 to + 150	$^{\circ}\text{C}$
Soldering Recommendations (Peak Temperature)		for 10 s			300 <sup>d</sup>	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$ , starting  $T_J = 25\text{ }^{\circ}\text{C}$ ,  $L = 2.7\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 18\text{ A}$  (see fig. 12).
- $I_{SD} \leq 20\text{ A}$ ,  $dI/dt \leq 150\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^{\circ}\text{C}$ .
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply


**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mounted, Steady-State) <sup>a</sup>	$R_{thJA}$	-	40	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.0	

**Note**

a. When mounted on 1" square PCB (FR-4 or G-10 material).

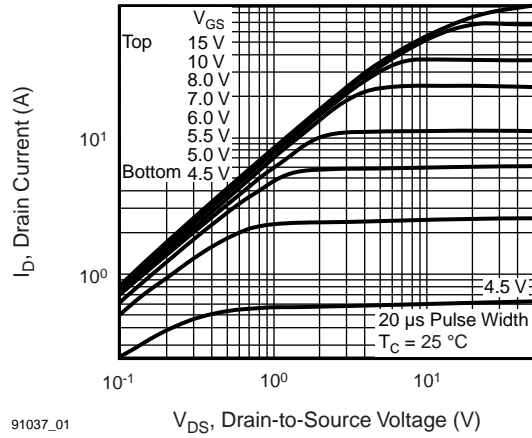
**SPECIFICATIONS** ( $T_J = 25\text{ °C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$		100	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}^c$		-	0.29	-	V/ $^\circ\text{C}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 200\text{ V}$ , $V_{GS} = 0\text{ V}$		-	-	25	$\mu\text{A}$
		$V_{DS} = 160\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ }^\circ\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 11\text{ A}^b$	-	0.020	-	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}$ , $I_D = 11\text{ A}^d$		6.7	-	-	S
Dynamic							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 25\text{ V}$ , $f = 1.0\text{ MHz}$ , see fig. 5 <sup>d</sup>		-	1300	-	pF
Output Capacitance	$C_{oss}$			-	430	-	
Reverse Transfer Capacitance	$C_{rss}$			-	130	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}$ , $V_{DS} = 160\text{ V}$ , see fig. 6 and 13 <sup>b, c</sup>	-	-	70	nC
Gate-Source Charge	$Q_{gs}$			-	-	13	
Gate-Drain Charge	$Q_{gd}$			-	-	39	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 100\text{ V}$ , $I_D = 20\text{ A}$ , $R_g = 9.1\text{ }\Omega$ , $R_D = 5.4\text{ }\Omega$ , see fig. 10 <sup>b, c</sup>		-	14	-	ns
Rise Time	$t_r$			-	51	-	
Turn-Off Delay Time	$t_{d(off)}$			-	45	-	
Fall Time	$t_f$			-	36	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	20	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	72	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_S = 20\text{ A}$ , $V_{GS} = 0\text{ V}^b$		-	-	2.0	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_F = 20\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}^{b, c}$		-	300	610	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	3.4	7.1	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

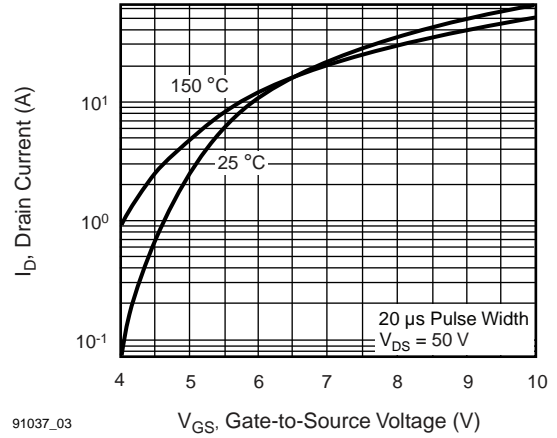
**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
 b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .  
 c. Uses IRF640/SiHF640 data and test conditions.

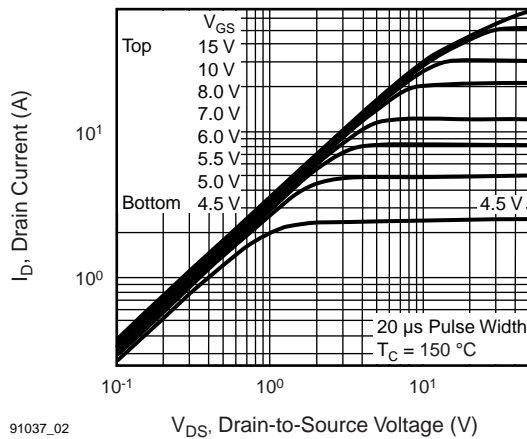
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



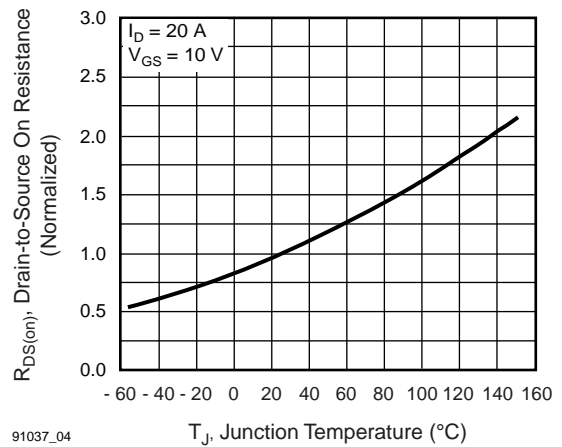
**Fig. 1 - Typical Output Characteristics,  $T_J = 25\text{ °C}$**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 2 - Typical Output Characteristics,  $T_J = 175\text{ °C}$**



**Fig. 4 - Normalized On-Resistance vs. Temperature**

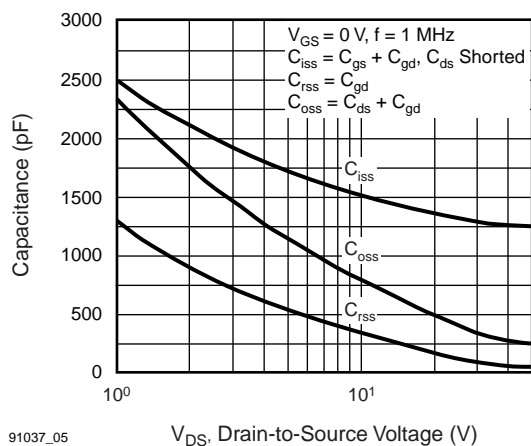


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

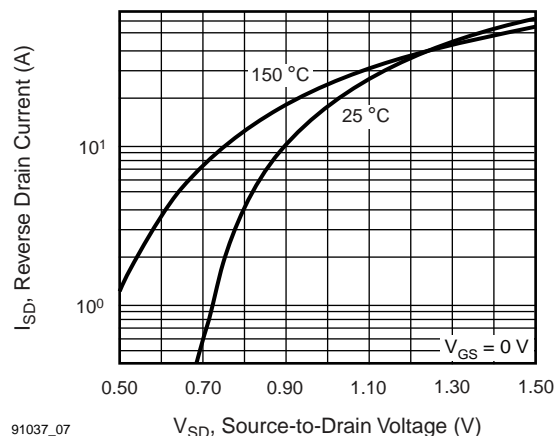


Fig. 7 - Typical Source-Drain Diode Forward Voltage

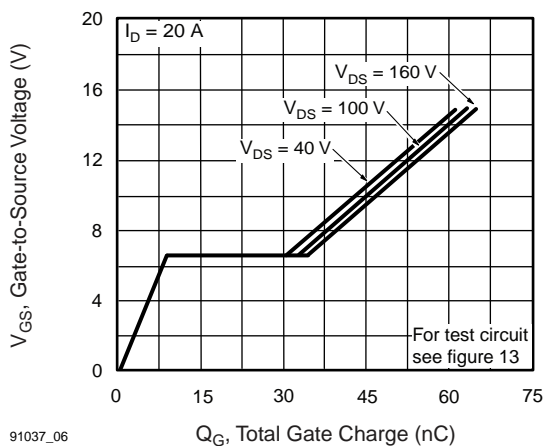


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

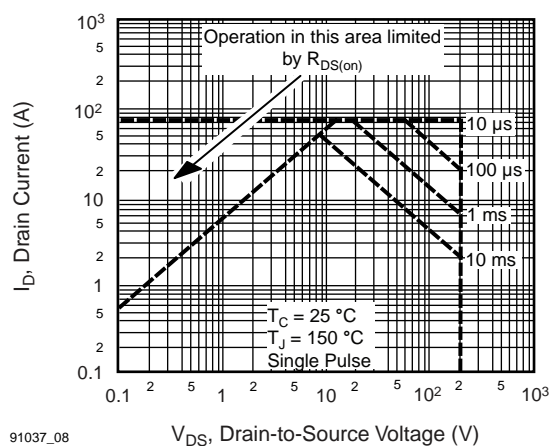
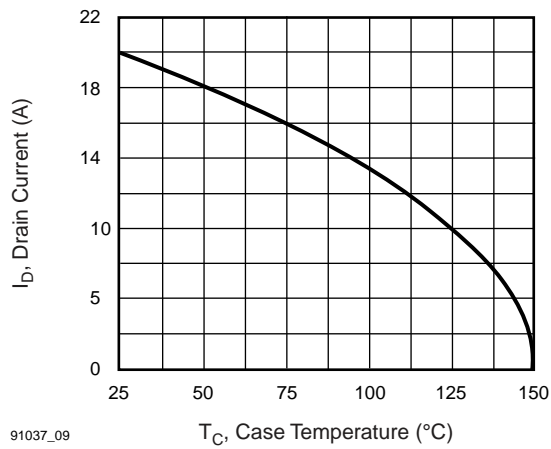
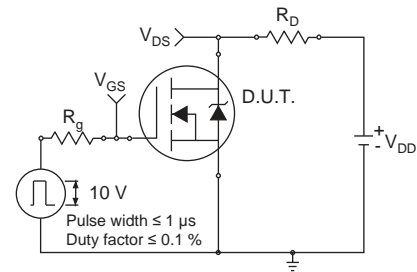


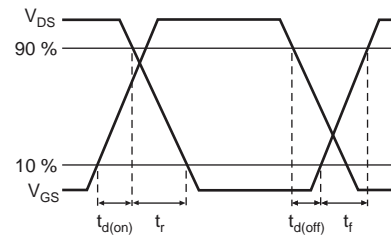
Fig. 8 - Maximum Safe Operating Area



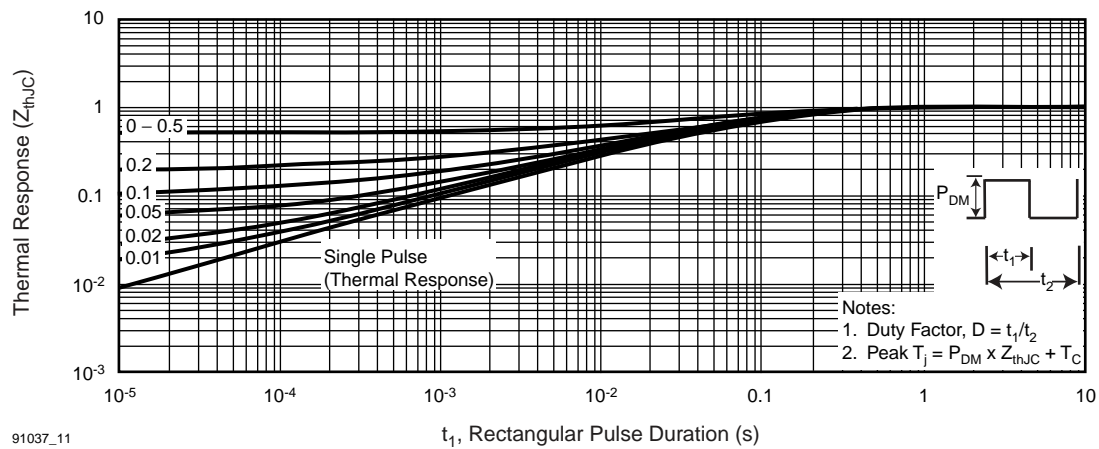
**Fig. 9 - Maximum Drain Current vs. Case Temperature**



**Fig. 10a - Switching Time Test Circuit**



**Fig. 10b - Switching Time Waveforms**



**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

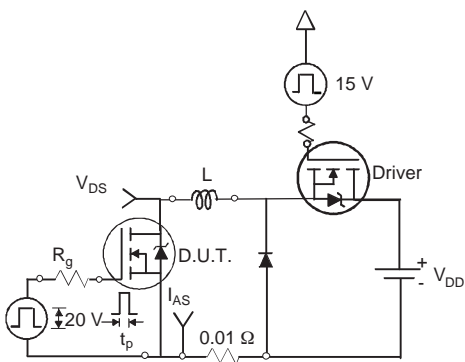


Fig. 12a - Unclamped Inductive Test Circuit

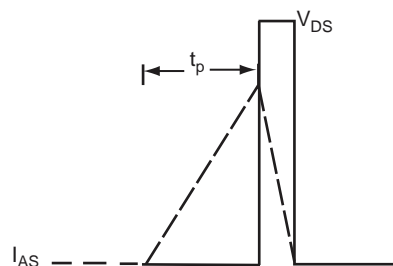


Fig. 12b - Unclamped Inductive Waveforms

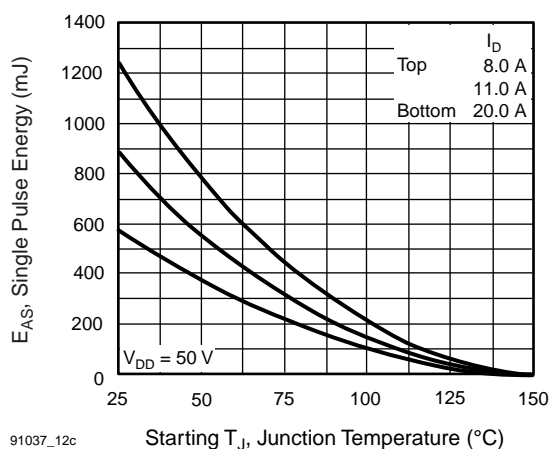


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

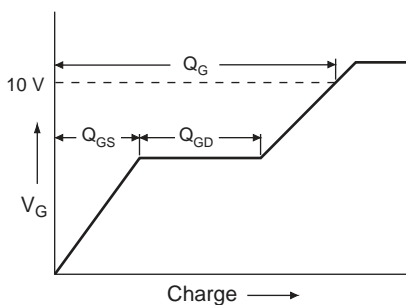


Fig. 13a - Basic Gate Charge Waveform

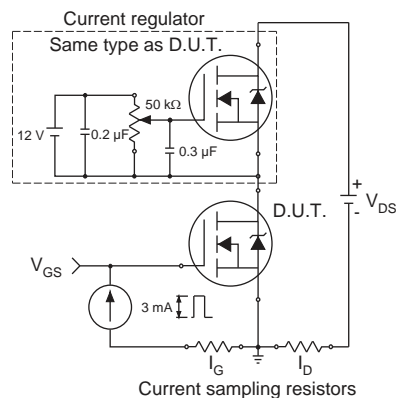
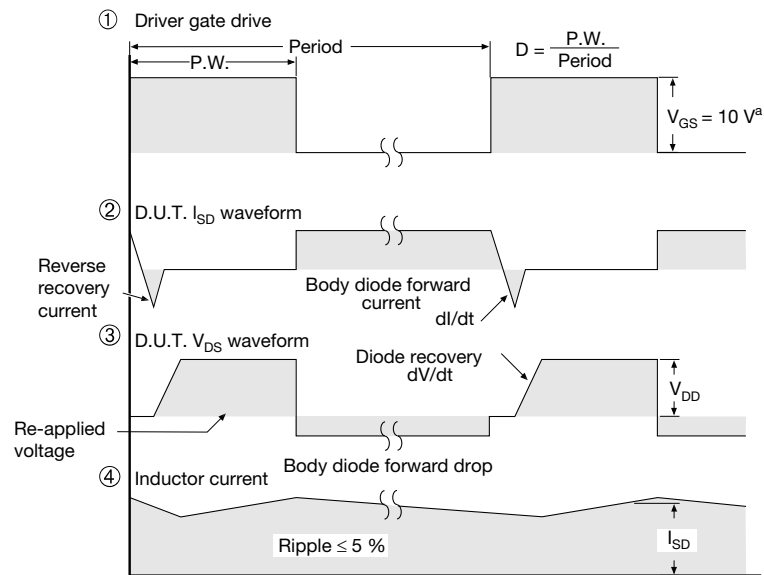
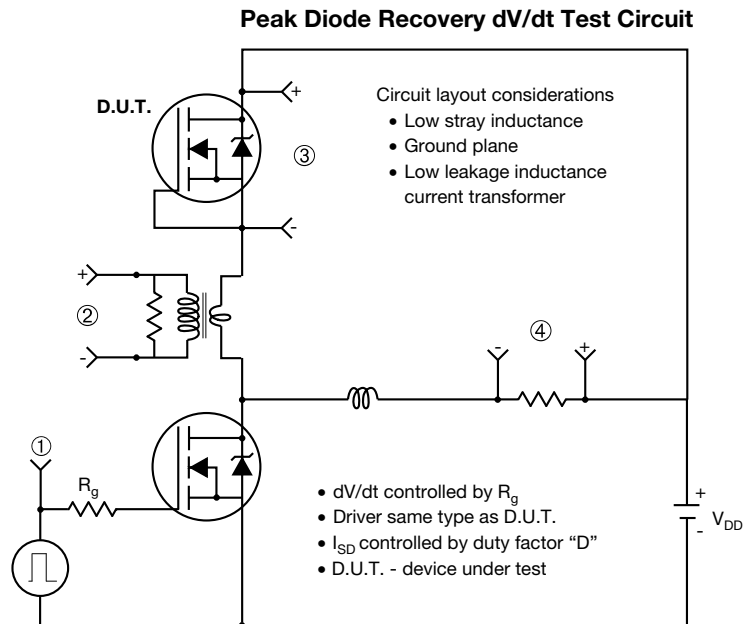


Fig. 13b - Gate Charge Test Circuit

**Note**a.  $V_{GS} = 5\text{ V}$  for logic level devices**Fig. 14 - For N-Channel**

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