

FSL38N20D-VB Datasheet N-Channel 200-V (D-S) MOSFET

PRODUCT SUMMARY					
V _{(BR)DSS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)	Q _g (Typ.)		
200	$0.038 \text{ at V}_{GS} = 15 \text{ V}$	45	57		
200	0.043 at V _{GS} = 10 V	40	57		

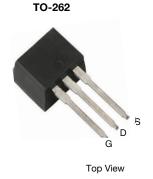
FEATURES

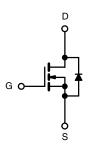
- Trench Power MOSFETS
- 175 °C Junction Temperature
- 100 % R_g and UIS Tested



APPLICATIONS

- Power Supply
- Lighting Systems





N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted						
Parameter		Symbol	Limit	Unit		
Drain-Source Voltage	e Voltage			V		
Gate-Source Voltage	V _{GS}	± 25	v			
Continuous Drain Current (T _J = 175 °C)	T _C = 25 °C	L	45			
	T _C = 100 °C	l _D	26	^		
Pulsed Drain Current	I _{DM}	150	— A			
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	20			
Single Pulse Avalanche Energy ^a	L = 0.111111	E _{AS}	20	mJ		
Maximum Power Dissipation ^a	T _C = 25 °C	В	166 ^b	14/		
	T _A = 25 °C ^c	P _D	3.12	W		
Operating Junction and Storage Temperature Ra	ange	T _J , T _{stg}	- 55 to 175	°C		

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Limit	Unit		
Junction-to-Ambient (PCB Mount) ^c	R_{thJA}	40	°C/W		
Junction-to-Case (Drain)	R_{thJC}	0.75	C/VV		

Notes:

- a. Duty cycle \leq 1 %.
- b. See SOA curve for voltage derating.
- c. When Mounted on 1" square PCB (FR-4 material).

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1



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static				<u>'</u>			
Drain-Source Breakdown Voltage	V _{(BR)DSS}	$V_{(BR)DSS}$ $V_{GS} = 0 \text{ V, } I_D = 250 \mu\text{A}$ 20					
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2.5		4.5	4.5 V	
Oats Ball I	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Gate-Body Leakage		$V_{DS} = 0 \text{ V}, V_{GS} = \pm 25 \text{ V}$			± 300		
		V _{DS} = 200 V, V _{GS} = 0 V			1		
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 200 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 100 ^{\circ}\text{C}$			25	μΑ	
		V _{DS} = 200 V, V _{GS} = 0 V, T _J = 150 °C			250		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	40			Α	
		V _{GS} = 10 V, I _D = 20 A		0.038		 	
	_	V _{GS} = 15 V, I _D = 20 A		0.043		Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A, T _J = 100 °C		0.088			
		V _{GS} = 10 V, I _D = 20 A, T _J = 150 °C		0.120		1	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 20 A	25			S	
Bynamie ^b				-			
Input Capacitance	C _{iss}			3100		pF	
Output Capacitance	C _{oss}	$V_{GS} = 0 \text{ V}, V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$		300			
Reverse Transfer Capacitance	C _{rss}			135			
Total Cata Charge	Qg	$V_{DS} = 100 \text{ V}, V_{GS} = 15 \text{ V}, I_D = 50 \text{ A}$		85	127		
Total Gate Charge ^c				57	85	200	
Gate-Source Charge ^c	Q_{gs}	$V_{DS} = 100 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 50 \text{ A}$		14		nC	
Gate-Drain Charge ^c	Q_{gd}			20			
Gate Resistance	R_{g}	f = 1 MHz		1.2	1.8	Ω	
Turn-On Delay Time ^c	t _{d(on)}			16	25		
Rise Time ^c	t _r	V_{DD} = 100 V, R_L = 2 Ω		170	260	no	
Turn-Off Delay Time ^c	t _{d(off)}	$I_D \cong 50 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		27	42	ns	
Fall Time ^c	t _f			9	18		
Seurce-Drain Dierle Fattingsann Cha	Pagrierisatic st						
Continuous Current	Is				36		
Pulsed Current	I _{SM}				80	A	
Forward Voltage ^a	V _{SD}	I _F = 20 A, V _{GS} = 0 V		0.86	1.5	V	
Reverse Recovery Time	t _{rr}			116	175	ns	
Peak Reverse Recovery Current	I _{RM(REC)}			9	14	Α	
Reverse Recovery Charge	Q _{rr}	$I_F = 40 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$		0.53	0.8	μC	
Reverse Recovery Fall Time	t _a	-		84		<u> </u>	
Reverse Recovery Rise Time	t _b			32		nS	

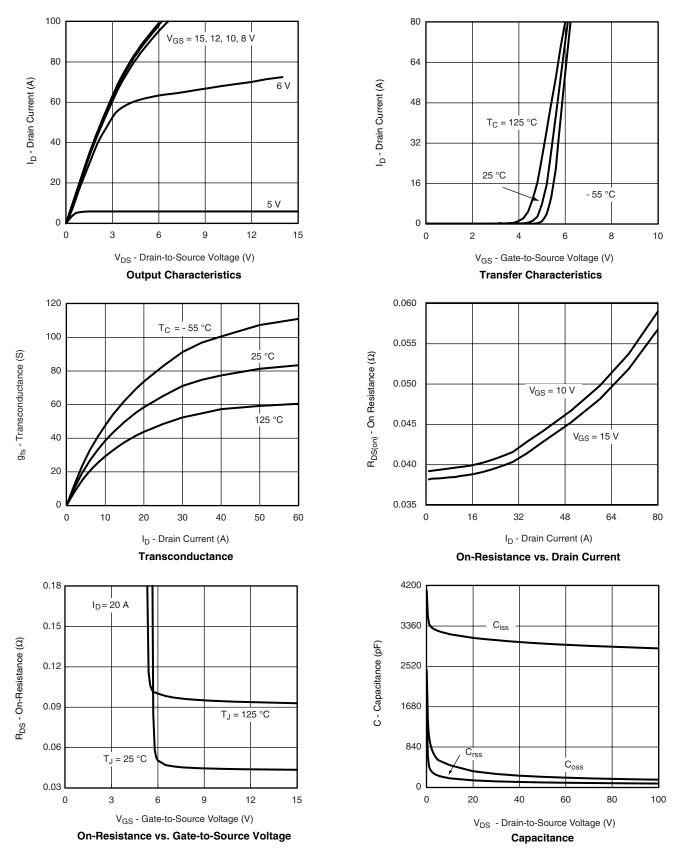
Notes:

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

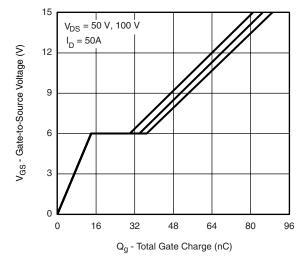


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

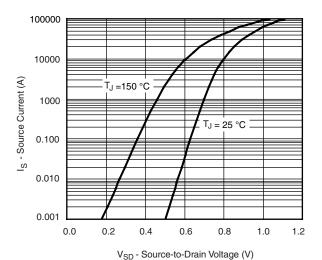




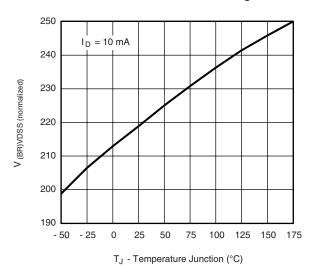
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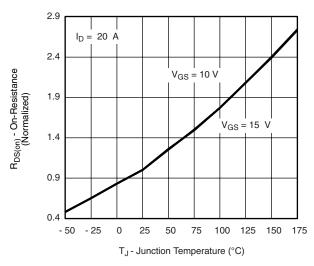
Gate Charge



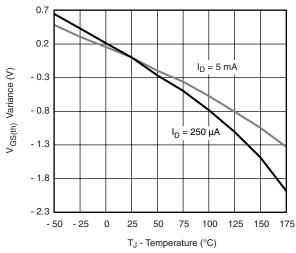
Source-Drain Diode Forward Voltage



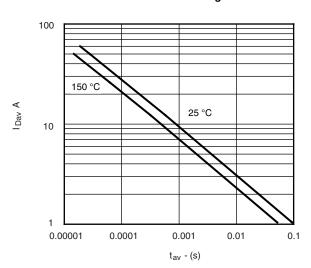
Drain Source Breakdown vs. Junction Temperature



On-Resistance vs. Junction Temperature



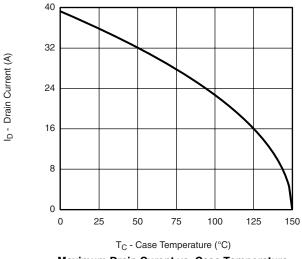
Threshold Voltage

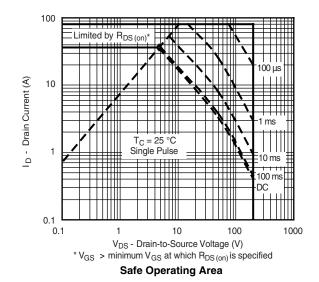


Single Pulse Avalanche Current Capability vs. Time

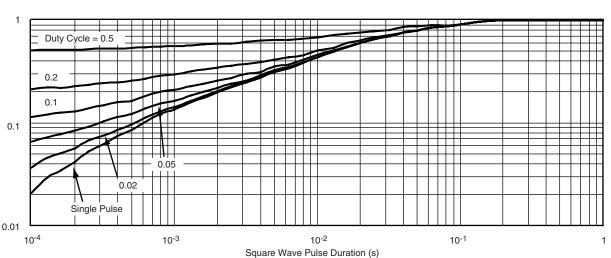


THERMAL RATINGS





Maximum Drain Curent vs. Case Temperature



Normalized Thermal Transient Impedance, Junction-to-Case

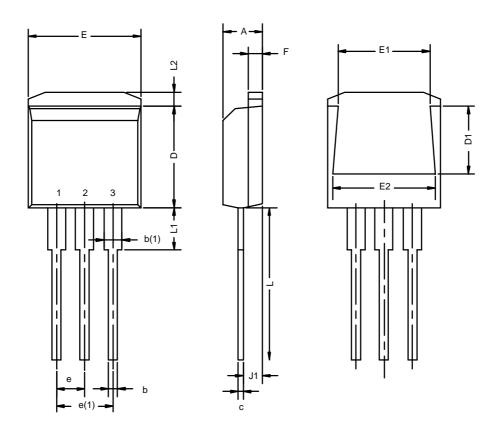
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Normalized Effective Transient Thermal Impedance

5



TO-262: 3-LEAD



	MILLIM	ETERS*	INCHES		
Dim	Min	Max	Min	Max	
Α	4.32	4.70	0.170	0.185	
b	0.64	1.00	0.025	0.039	
b(1)	1.14	1.40	0.045	0.055	
С	0.36	0.50	0.014	0.020	
D	8.64	9.65	0.340	0.380	
D1	5.59	6.10	0.220	0.240	
е	2.41	2.67	0.095	0.105	
e(1)	4.95	5.33	0.195	0.210	
E	10.03	10.41	0.395	0.410	
E1	7.87	8.64	0.310	0.340	
E2	9.02	9.53	0.355	0.375	
F	1.14	1.40	0.045	0.055	
J1	2.41	2.79	0.095	0.110	
L	13.08	14.22	0.515	0.560	
L1	-	3.81	-	0.150	
L2	1.02	1.40	0.040	0.055	
ECN: T-02234—Rev. C, 14-Oct-02 DWG: 5855					

^{*}Use millimeters as the primary measurement



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