

## AUIRFZ44NL-VB Datasheet

### Power MOSFET

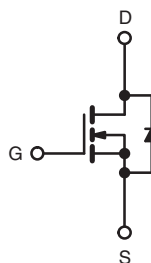
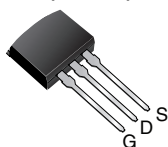
PRODUCT SUMMARY		
$V_{DS}$ (V)	60	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	0.015
$Q_g$ (Max.) (nC)	110	
$Q_{gs}$ (nC)	29	
$Q_{gd}$ (nC)	36	
Configuration	Single	

#### FEATURES

- Advanced process technology
- 175 °C operating temperature
- Fast switching



I<sup>2</sup>PAK (TO-262)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V <sub>DS</sub>	60	V
Gate-Source Voltage			V <sub>GS</sub>	± 20	
Continuous Drain Current <sup>f</sup>	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	I <sub>D</sub>	60	A
		T <sub>C</sub> = 100 °C		50	
Pulsed Drain Current <sup>a, e</sup>			I <sub>DM</sub>	290	
Linear Derating Factor				1.3	W/°C
Single Pulse Avalanche Energy <sup>b, e</sup>			E <sub>AS</sub>	100	mJ
Maximum Power Dissipation	T <sub>C</sub> = 25 °C		P <sub>D</sub>	190	W
	T <sub>A</sub> = 25 °C			3.7	
Peak Diode Recovery dV/dt <sup>c, e</sup>			dV/dt	4.5	V/ns
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Soldering Recommendations (Peak temperature) <sup>d</sup>	for 10 s			300	


#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25\text{ V}$ , Starting  $T_J = 25\text{ }^{\circ}\text{C}$ ,  $L = 22\text{ }\mu\text{H}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 72\text{ A}$  (see fig. 12).
- $I_{SP} \leq 72\text{ A}$ ,  $dI/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 175\text{ }^{\circ}\text{C}$ .
- 1.6 mm from case.
- Uses IRFZ48, SiHFZ48 data and test conditions.
- Calculated continuous current based on maximum allowable junction temperature.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB mount) <sup>a</sup>	$R_{thJA}$	-	40	°C / W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.8	

**Note**

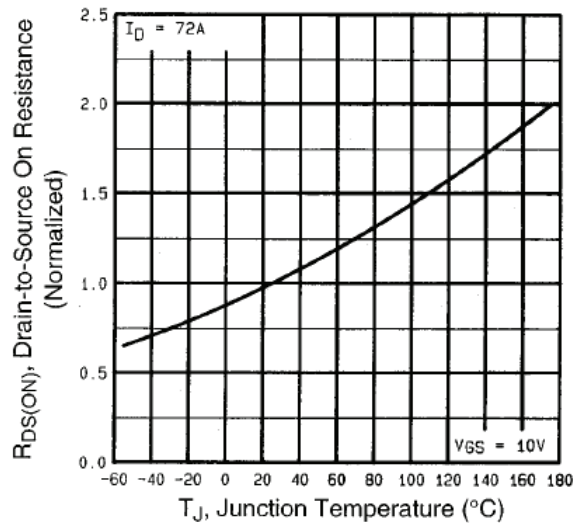
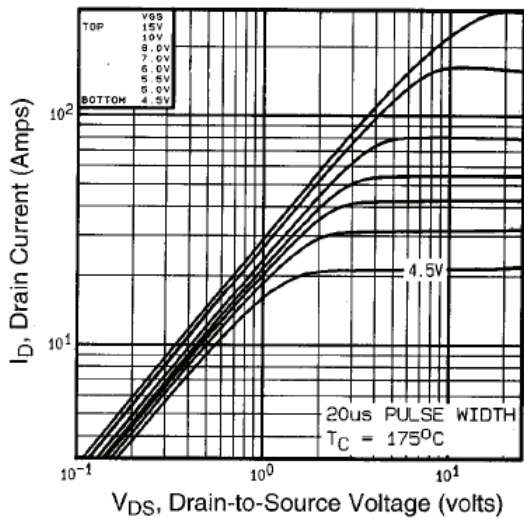
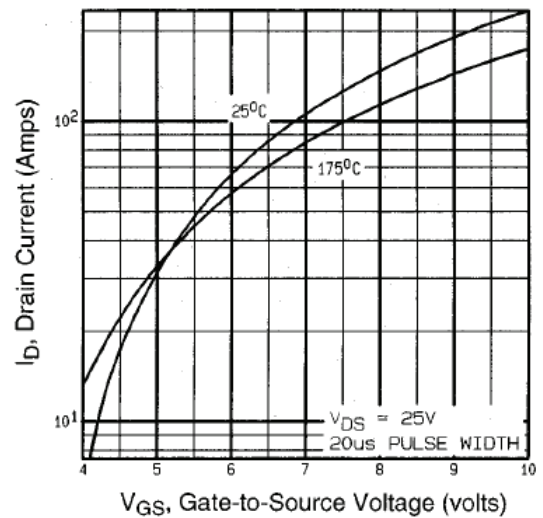
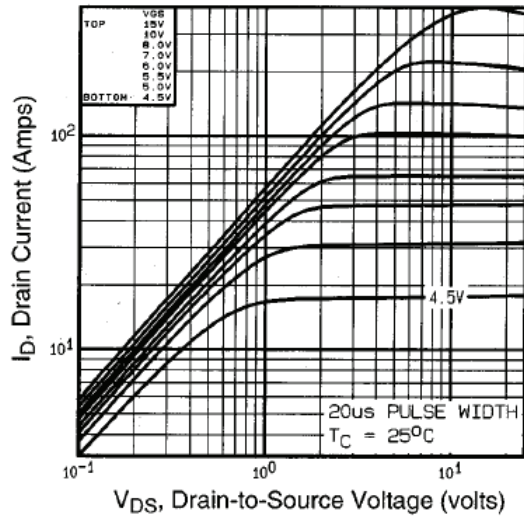
a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0, I <sub>D</sub> = 250 μA		60	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA <sup>c</sup>		-	0.060	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		1.5	-	3.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V		-	-	25	μA
		V <sub>DS</sub> = 48 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 150 °C		-	-	250	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 15 A <sup>b</sup>	-	0.015	-	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 25 V, I <sub>D</sub> = 15 A <sup>b</sup>		27	-	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5 <sup>c</sup>		-	3500	-	pF
Output Capacitance	C <sub>oss</sub>			-	1300	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	190	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 12 A, V <sub>DS</sub> = 48 V, see fig. 6 and 13 <sup>b, c</sup>	-	-	110	nC
Gate-Source Charge	Q <sub>gs</sub>			-	-	29	
Gate-Drain Charge	Q <sub>gd</sub>			-	-	36	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 12 A, R <sub>g</sub> = 9.1 Ω, R <sub>D</sub> = 0.34 Ω, see fig. 10 <sup>b, c</sup>		-	8.1	-	ns
Rise Time	t <sub>r</sub>			-	250	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	210	-	
Fall Time	t <sub>f</sub>			-	250	-	
Internal Source Inductance	L <sub>S</sub>	Between lead, and center of die contact		-	7.5	-	nH
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	50 <sup>c</sup>	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	90	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 72 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	2.0	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 72 A, dI/dt = 100 A/μs <sup>b, c</sup>		-	120	180	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	500	800	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

**Notes**

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- Uses VBL1615/AUIRFZ44NL-VB data and test conditions.
- Calculated continuous current based on maximum allowable junction temperature.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



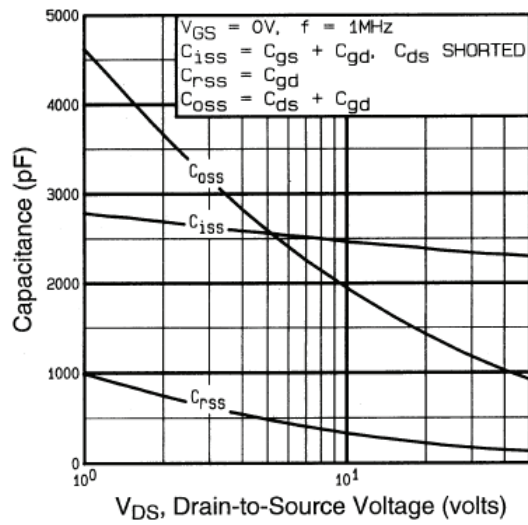


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

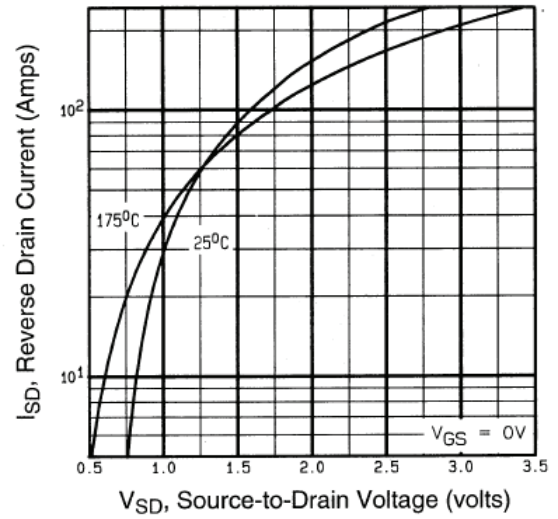


Fig. 7 - Typical Source-Drain Diode Forward Voltage

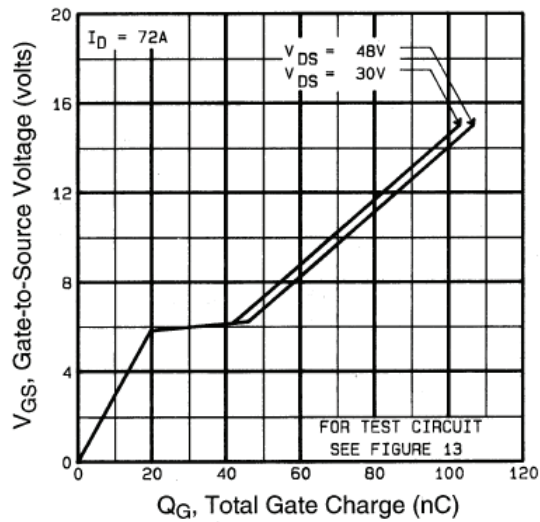


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

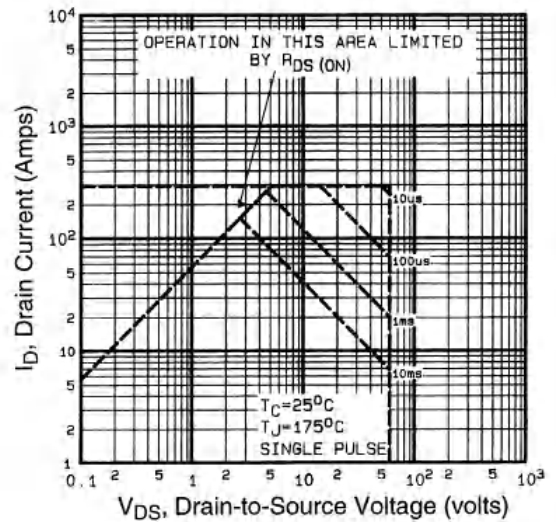


Fig. 8 - Maximum Safe Operating Area

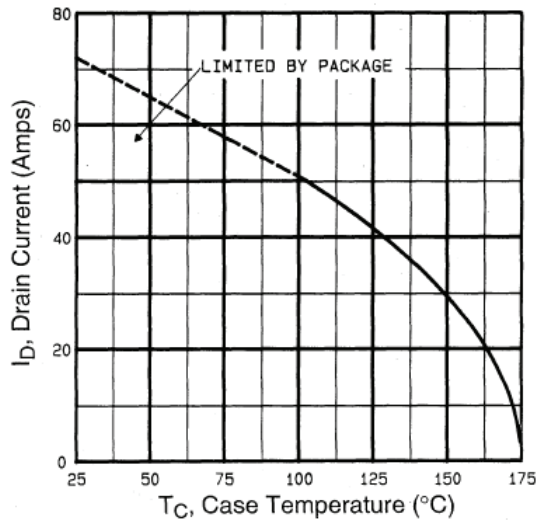


Fig. 9 - Maximum Drain Current vs. Case Temperature

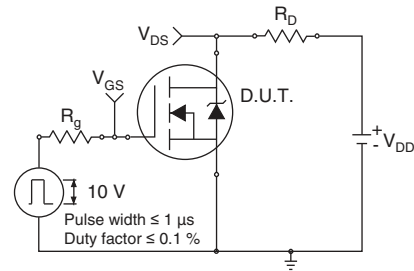


Fig. 10a - Switching Time Test Circuit

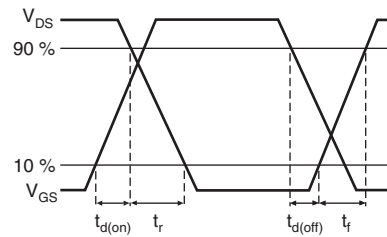


Fig. 10b - Switching Time Waveform

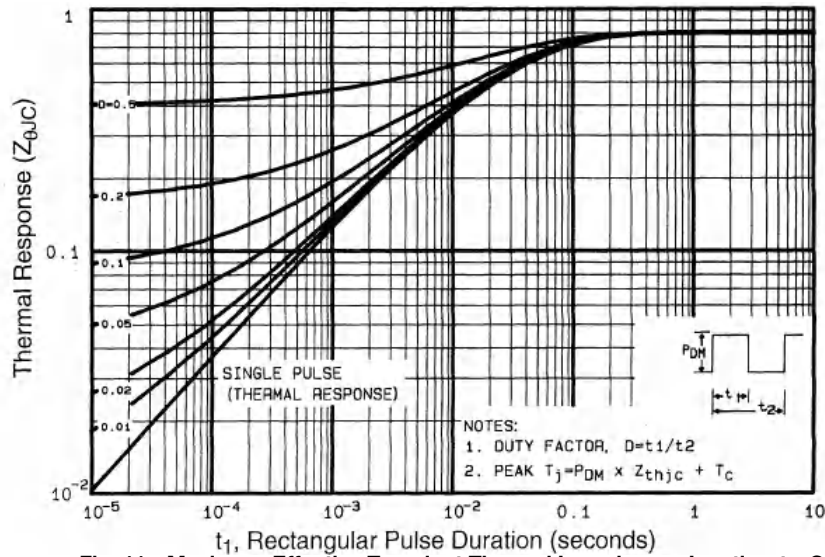


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

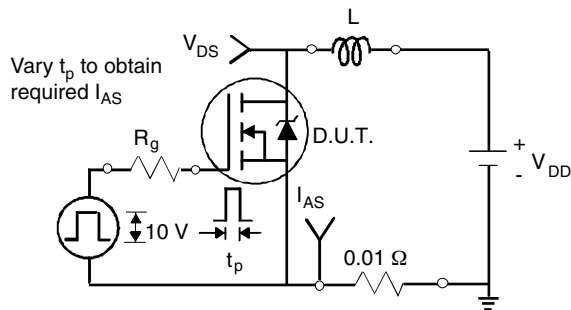


Fig. 12a - Unclamped Inductive Test Circuit

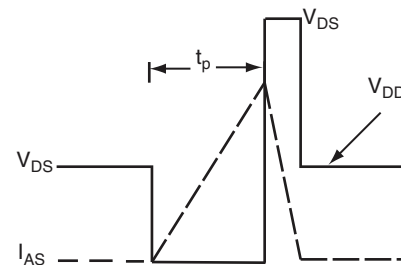


Fig. 12b - Unclamped Inductive Waveforms

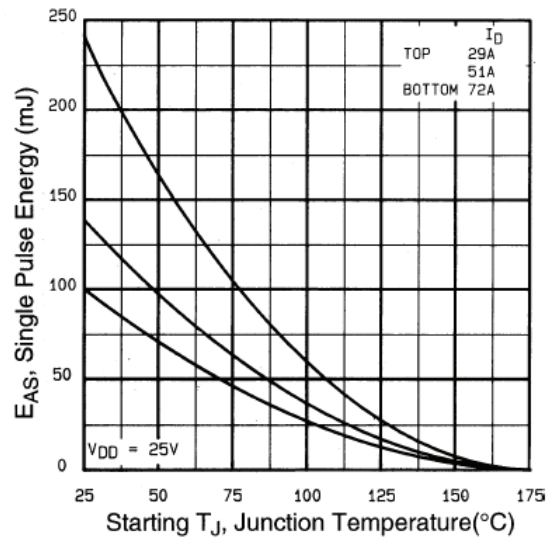


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

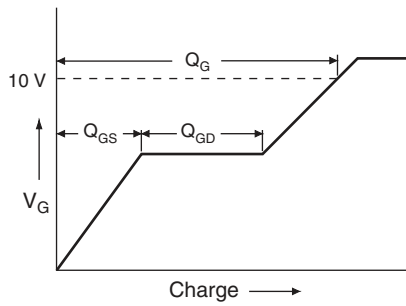


Fig. 13a - Maximum Avalanche Energy vs. Drain Current

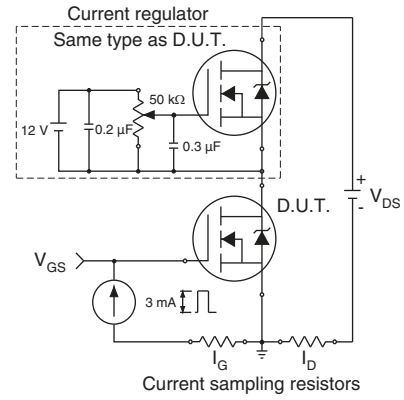
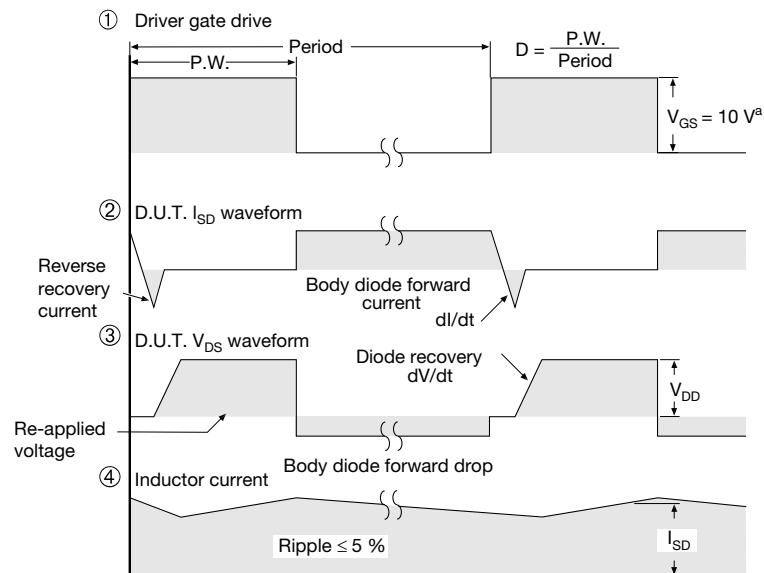
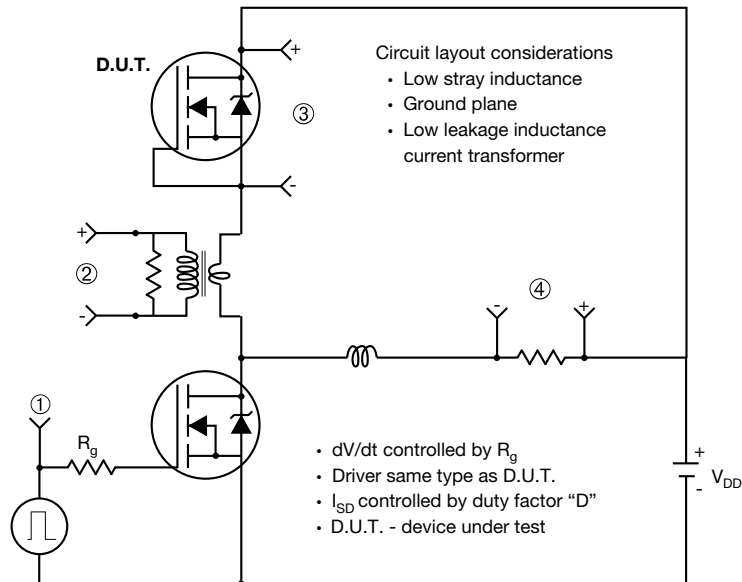


Fig. 13b - Gate Charge Test Circuit

### Peak Diode Recovery dV/dt Test Circuit

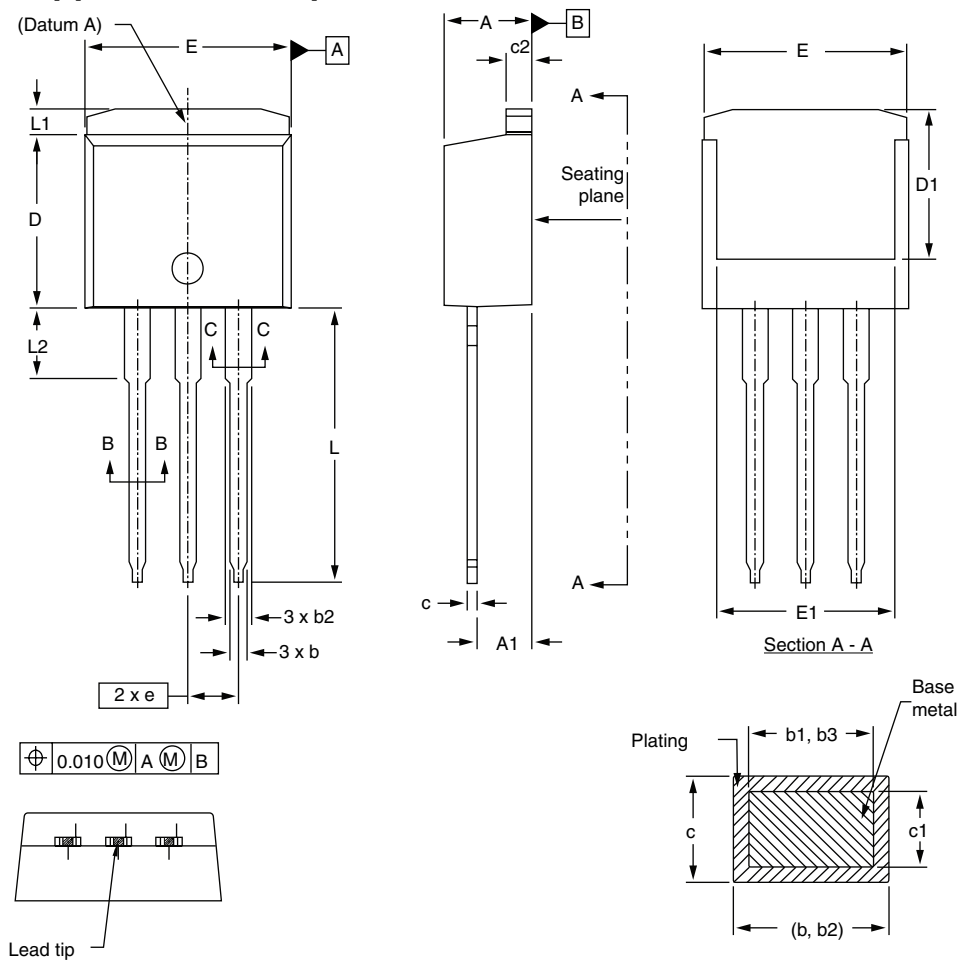


**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

## I<sup>2</sup>PAK (TO-262) (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	2.03	3.02	0.080	0.119
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D	8.38	9.65	0.330	0.380
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
L	13.46	14.10	0.530	0.555
L1	-	1.65	-	0.065
L2	3.56	3.71	0.140	0.146

ECN: S-82442-Rev. A, 27-Oct-08  
DWG: 5977

### Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outmost extremes of the plastic body.
3. Thermal pad contour optional within dimension E, L1, D1, and E1.
4. Dimension b1 and c1 apply to base metal only.



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