

ZXMP10A18KTC-VB Datasheet

P-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
- 100	0.250 at $V_{GS} = - 10$ V	- 8.8	11.7
	0.280 at $V_{GS} = - 4.5$ V	- 8.0	

FEATURES

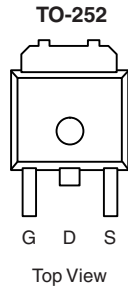
- Halogen-free According to IEC 61249-2-21 Definition
- Trench Power MOSFET
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



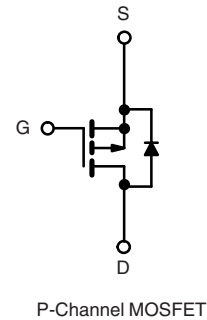
RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Power Switch
- DC/DC Converters



Drain Connected to Tab



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 100	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	I_D	$T_C = 25^\circ\text{C}$ - 8.8	A
		$T_C = 70^\circ\text{C}$ - 7.1	
Pulsed Drain Current	I_{DM}	- 25	
Avalanche Current	I_{AS}	- 18	mJ
Single Avalanche Energy ^a	E_{AS}	16.2	
Maximum Power Dissipation ^a	P_D	$T_C = 25^\circ\text{C}$ 32.1 ^b	W
		$T_A = 25^\circ\text{C}^c$ 2.5	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mount) ^c	R_{thJA}	50	$^\circ\text{C/W}$
Junction-to-Case (Drain)	R_{thJC}	3.9	

Notes:

a. Duty cycle $\leq 1\%$.

b. See SOA curve for voltage derating.

c. When Mounted on 1" square PCB (FR-4 material).

SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{DS} = 0 V, I _D = - 250 μA	- 100			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 1		- 2.5	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 250	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 100 V, V _{GS} = 0 V			- 1	μA
		V _{DS} = - 100 V, V _{GS} = 0 V, T _J = 125 °C			- 50	
		V _{DS} = - 100 V, V _{GS} = 0 V, T _J = 150 °C			- 250	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ - 10 V, V _{GS} = - 10 V	- 15			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 10 V, I _D = - 3.6 A		0.250		Ω
		V _{GS} = - 4.5 V, I _D = - 3.4 A		0.280		
Forward Transconductance ^a	g _{fs}	V _{DS} = - 15 V, I _D = - 3.6 A		12		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = - 50 V, f = 1 MHz		1055		pF
Output Capacitance	C _{oss}			65		
Reverse Transfer Capacitance	C _{rss}			41		
Total Gate Charge ^c	Q _g	V _{DS} = - 50 V, V _{GS} = - 10 V, I _D = - 3.6 A		23.2	34.8	nC
Gate-Source Charge ^c	Q _{gs}	V _{DS} = - 50 V, V _{GS} = - 4.5 V, I _D = - 3.6 A		11.7	17.6	
Gate-Drain Charge ^c	Q _{gd}			3.5		
Gate Resistance	R _g	f = 1 MHz	1.2	5.7	11.5	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = - 50 V, R _L = 17.2 Ω I _D ≅ - 2.9 A, V _{GEN} = - 10 V, R _g = 1 Ω		7	14	ns
Rise Time ^c	t _r			12	18	
Turn-Off Delay Time ^c	t _{d(off)}			33	50	
Fall Time ^c	t _f			9	18	
Drain-Source Body Diode Ratings and Characteristics T _C = 25 °C ^b						
Continuous Current	I _S				- 8.8	A
Pulsed Current	I _{SM}				- 15	
Forward Voltage ^a	V _{SD}	I _F = - 2.9 A, V _{GS} = 0 V		- 0.8	- 1.5	V
Reverse Recovery Time	t _{rr}	I _F = - 2.9 A, dI/dt = 100 A/μs		50	75	ns
Peak Reverse Recovery Current	I _{RM(REC)}			- 4	- 6	A
Reverse Recovery Charge	Q _{rr}			98	147	nC

Notes:

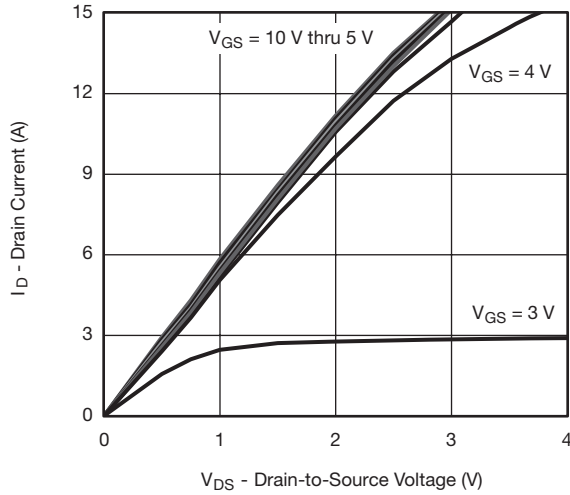
a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

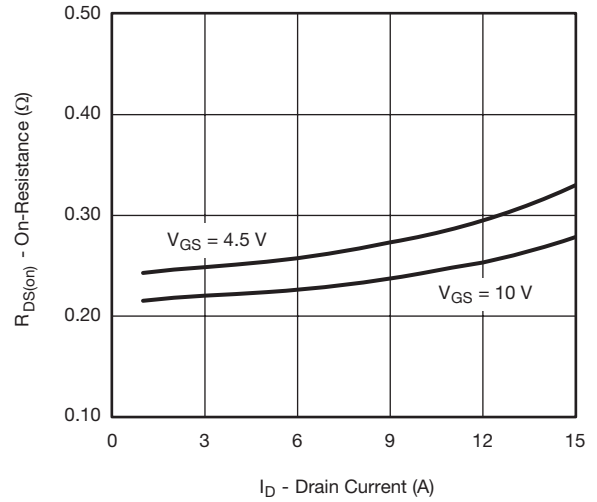
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

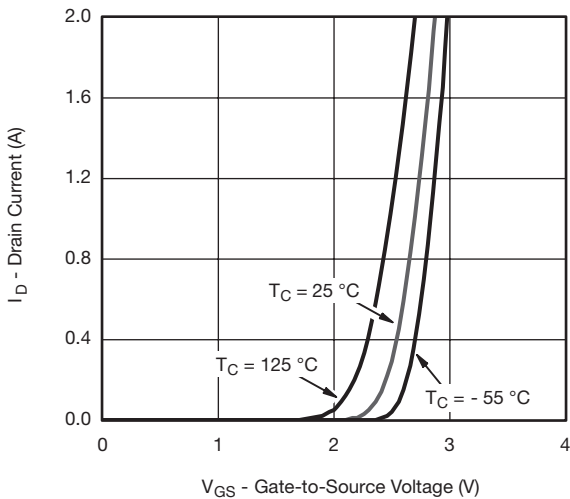
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



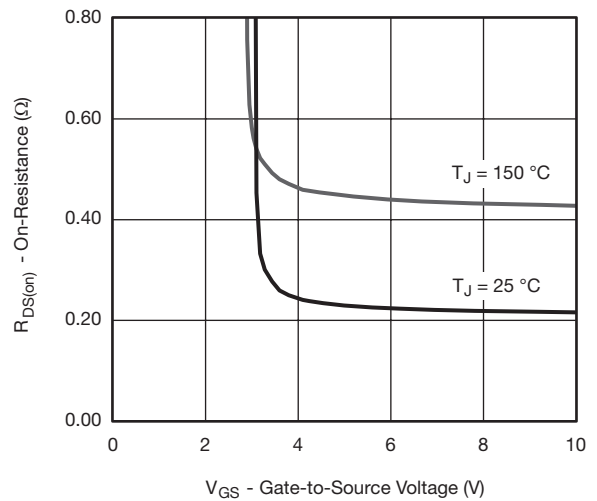
Output Characteristics



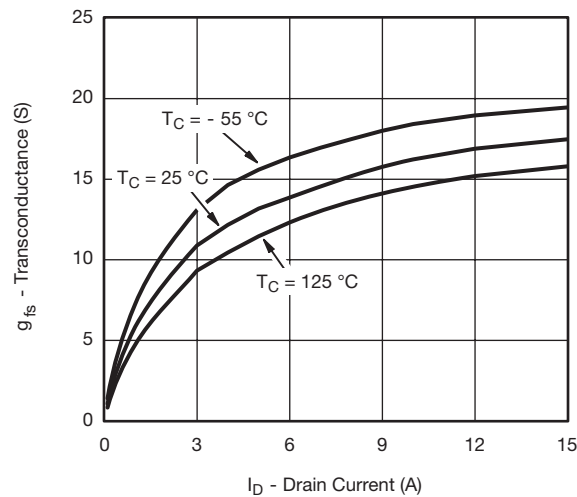
On-Resistance vs. Drain Current



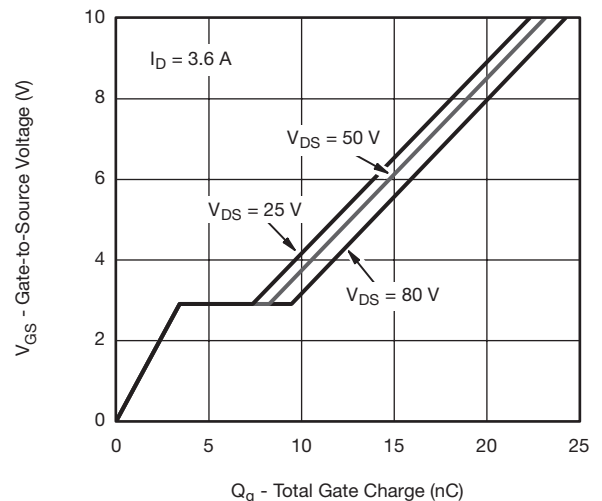
Transfer Characteristics



On-Resistance vs. Gate-to-Source Voltage

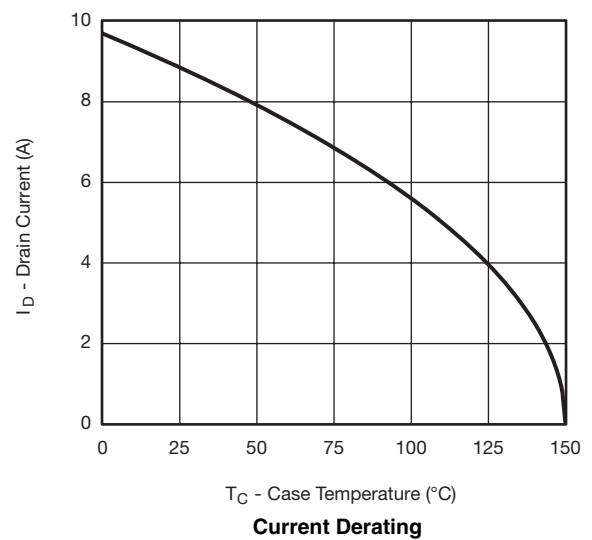
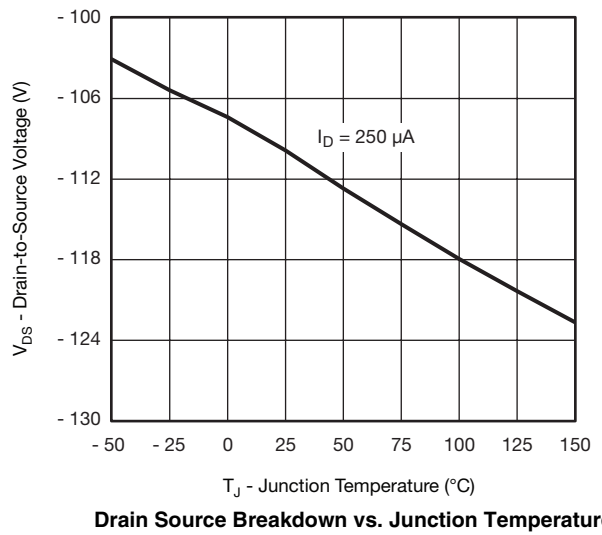
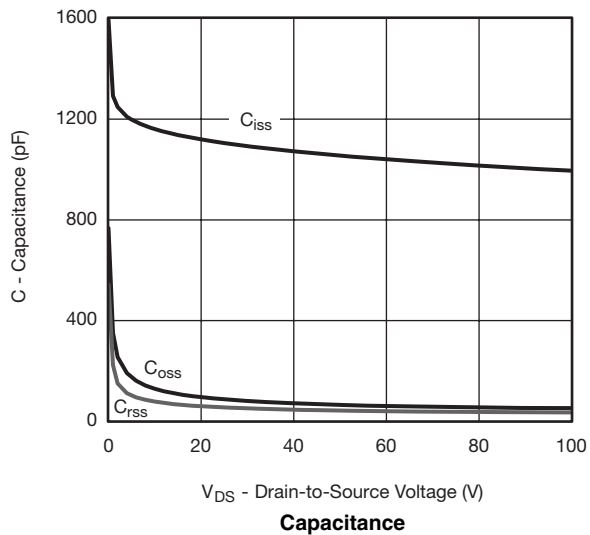
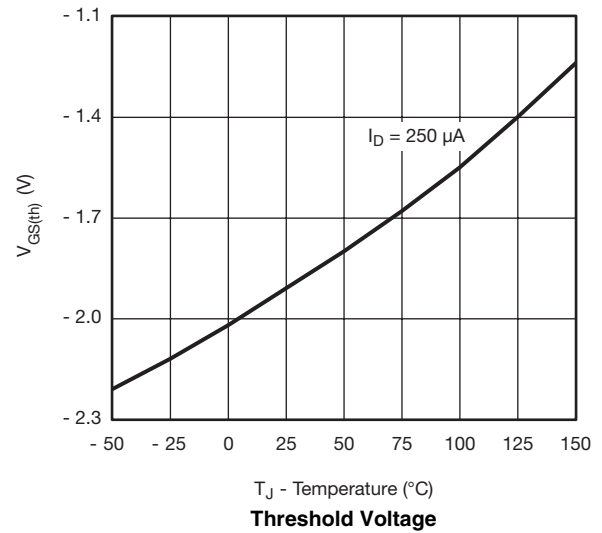


Transconductance

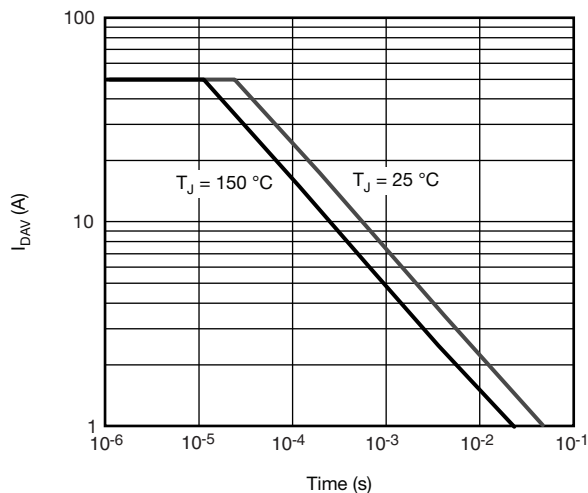


Gate Charge

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

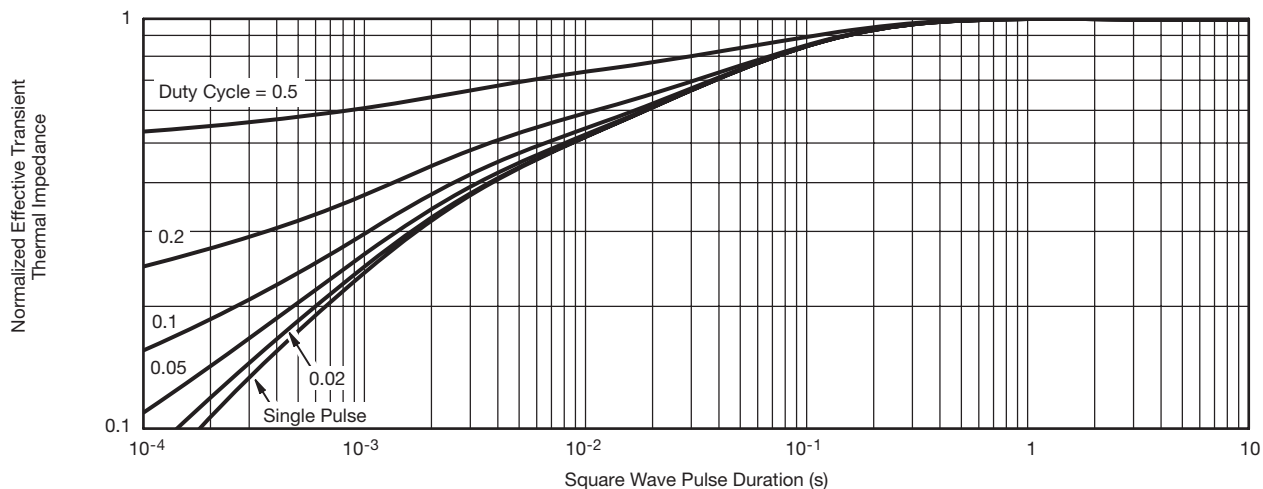


Single Pulse Avalanche Current Capability vs. Time



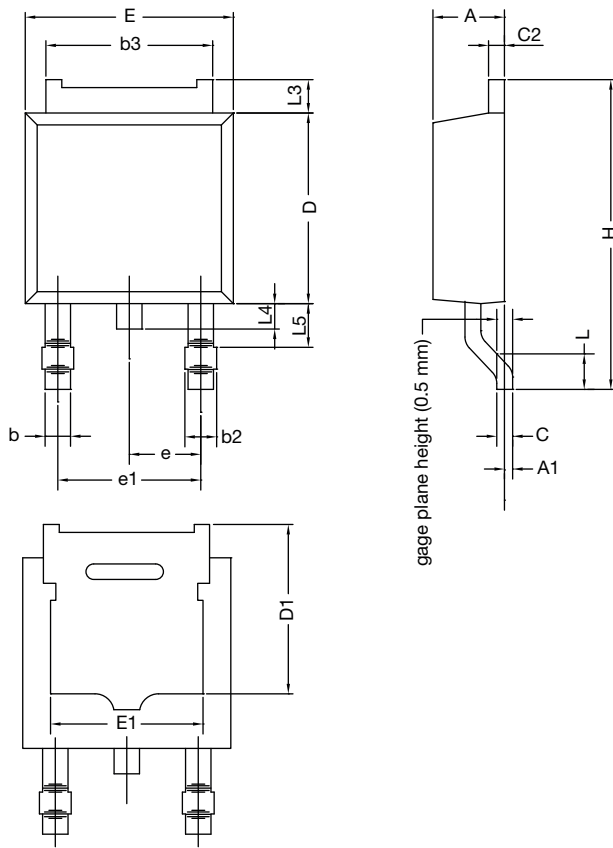
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

TO-252AA Case Outline



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T16-0236-Rev. P, 16-May-16 DWG: 5347				

Notes

- Dimension L3 is for reference only.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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