

# SWD3N80D-VB Datasheet

## N-Channel 800V (D-S) Super Junction Power MOSFET



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### PRODUCT SUMMARY

$V_{DS}$ (V) at $T_J$ max.	800	
$R_{DS(on)}$ typ. ( $\Omega$ ) at 25 °C	$V_{GS} = 10$ V	2.38
$Q_g$ max. (nC)	90	
$Q_{gs}$ (nC)	11	
$Q_{gd}$ (nC)	19	
Configuration	Single	

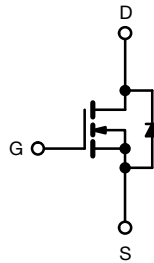
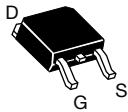
### FEATURES

- Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low input capacitance ( $C_{iss}$ )
- Reduced switching and conduction losses
- Ultra low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)

### APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Renewable energy
  - Solar (PV inverters)

**DPAK**  
(TO-252)



N-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			$V_{DS}$	800	V
Gate-source voltage			$V_{GS}$	$\pm 30$	
Continuous drain current ( $T_J = 150\text{ }^{\circ}\text{C}$ )	$V_{GS}$ at 10 V	$T_C = 25\text{ }^{\circ}\text{C}$	$I_D$	2.8	A
		$T_C = 100\text{ }^{\circ}\text{C}$		1.8	
Pulsed drain current <sup>a</sup>			$I_{DM}$	5	
Linear derating factor				0.5	W/ $^{\circ}\text{C}$
Single pulse avalanche energy <sup>b</sup>			$E_{AS}$	14	mJ
Maximum power dissipation			$P_D$	62.5	W
Operating junction and storage temperature range			$T_J, T_{stg}$	-55 to +150	$^{\circ}\text{C}$
Drain-source voltage slope	$T_J = 125\text{ }^{\circ}\text{C}$		$dV/dt$	70	V/ns
Reverse diode $dV/dt$ <sup>d</sup>		0.13			
Soldering recommendations (peak temperature) <sup>c</sup>	For 10 s			300	$^{\circ}\text{C}$


#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 140$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 0.9$  A
- 1.6 mm from case
- $I_{SD} \leq I_D$ ,  $dI/dt = 100$  A/ $\mu$ s, starting  $T_J = 25$  °C

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	62	°C/W
Maximum junction-to-case (drain)	$R_{thJC}$	-	2.0	

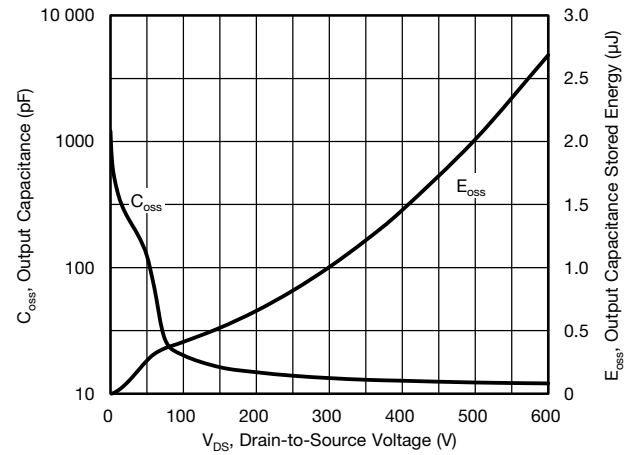
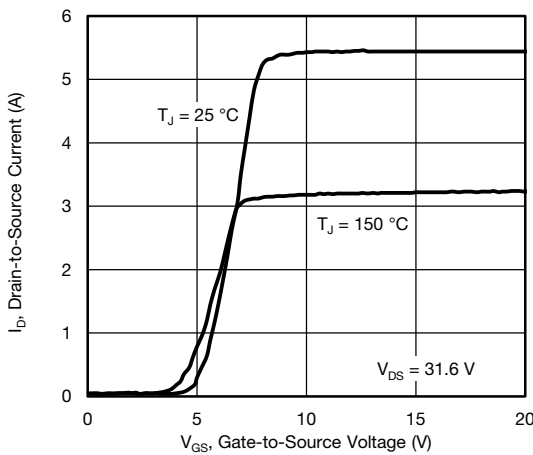
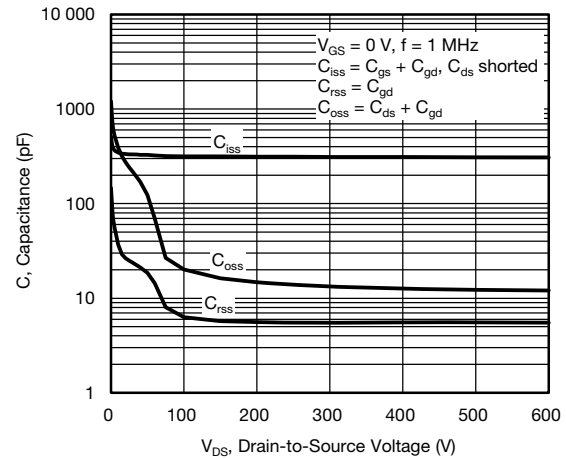
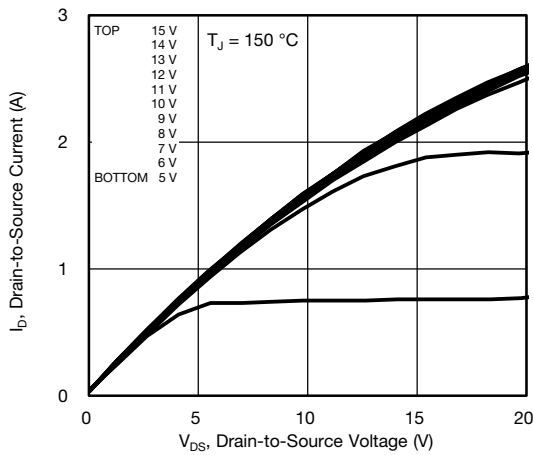
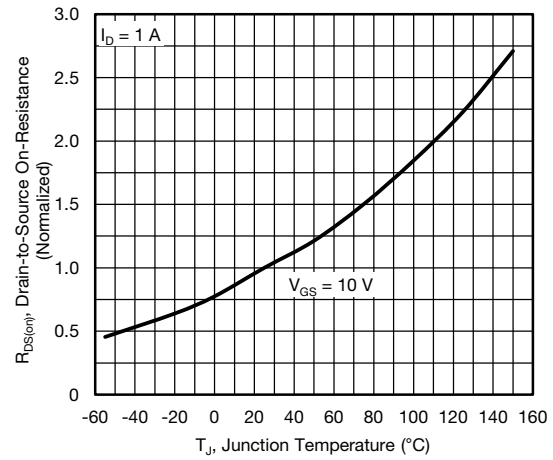
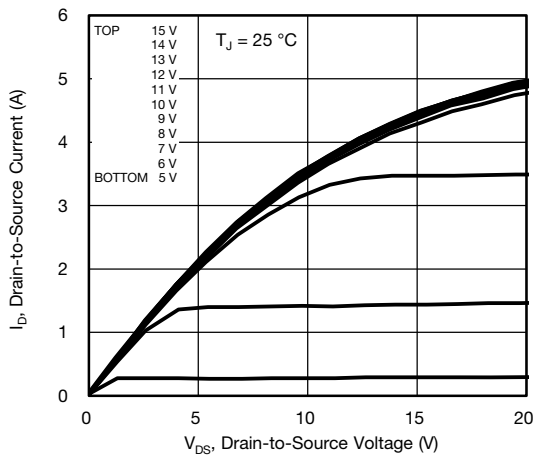
**SPECIFICATIONS** ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		800	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	1.0	-	V/°C
Gate-source threshold Voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
		V <sub>GS</sub> = ± 30 V		-	-	± 1	μA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 800 V, V <sub>GS</sub> = 0 V		-	-	1	μA
		V <sub>DS</sub> = 640 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	10	
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 1.0 A	-	2.38	-	Ω
Forward transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 1.0 A		-	1.0	-	S
Dynamic							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 100 V, f = 1 MHz		-	315	-	pF
Output capacitance	C <sub>Oss</sub>			-	20	-	
Reverse transfer capacitance	C <sub>rss</sub>			-	6	-	
Effective output capacitance, energy related <sup>a</sup>	C <sub>O(er)</sub>	V <sub>DS</sub> = 0 V to 480 V, V <sub>GS</sub> = 0 V		-	13	-	
Effective output capacitance, time related <sup>b</sup>	C <sub>O(tr)</sub>			-	45	-	
Total gate charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 1.0 A, V <sub>DS</sub> = 480 V	-	9.8	19.6	nC
Gate-source charge	Q <sub>gs</sub>			-	2.4	-	
Gate-drain charge	Q <sub>gd</sub>			-	3.9	-	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 480 V, I <sub>D</sub> = 1.0 A, V <sub>GS</sub> = 10 V, R <sub>g</sub> = 9.1 Ω		-	11	22	ns
Rise time	t <sub>r</sub>			-	7	14	
Turn-off delay time	t <sub>d(off)</sub>			-	19	38	
Fall time	t <sub>f</sub>			-	27	54	
Gate input resistance	R <sub>g</sub>	f = 1 MHz, open drain		1.8	3.6	7.2	Ω
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	2.8	A
Pulsed diode forward current	I <sub>SM</sub>			-	-	5	
Diode forward voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 11 A, V <sub>GS</sub> = 0 V		-	-	1.2	V
Reverse recovery time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = I <sub>S</sub> = 1.0 A, dI/dt = 100 A/μs, V <sub>R</sub> = 25 V		-	278	556	ns
Reverse recovery charge	Q <sub>rr</sub>			-	0.9	1.8	μC
Reverse recovery current	I <sub>RRM</sub>			-	5	-	A

**Notes**

- a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$   
 b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



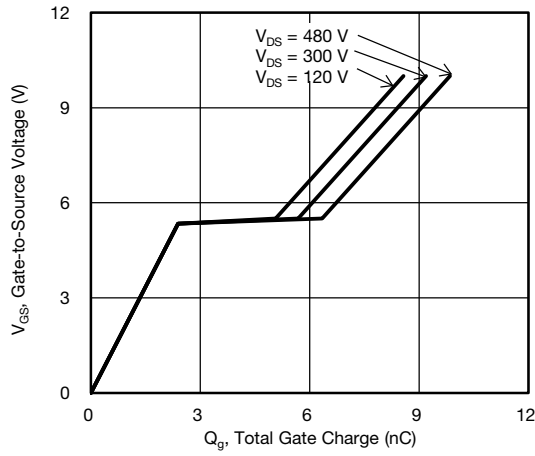


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

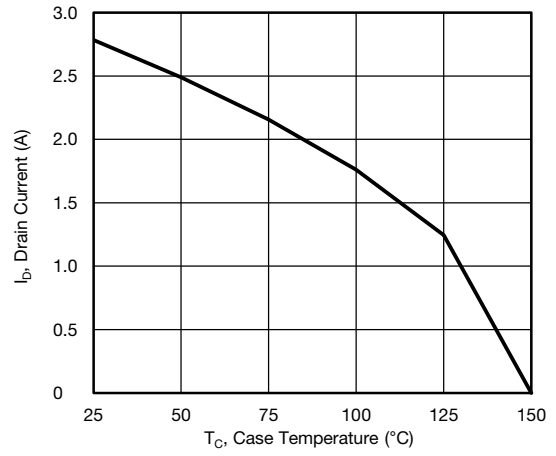


Fig. 10 - Maximum Drain Current vs. Case Temperature

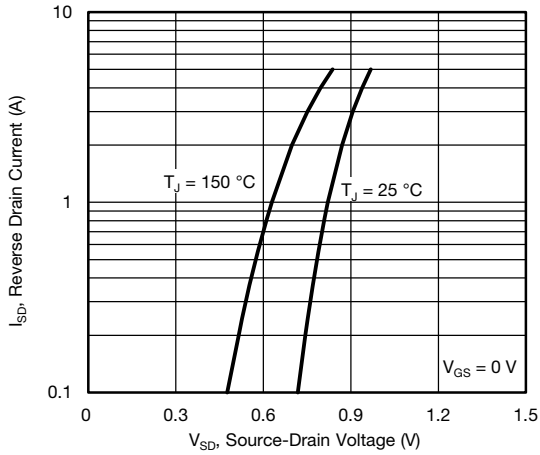


Fig. 8 - Typical Source-Drain Diode Forward Voltage

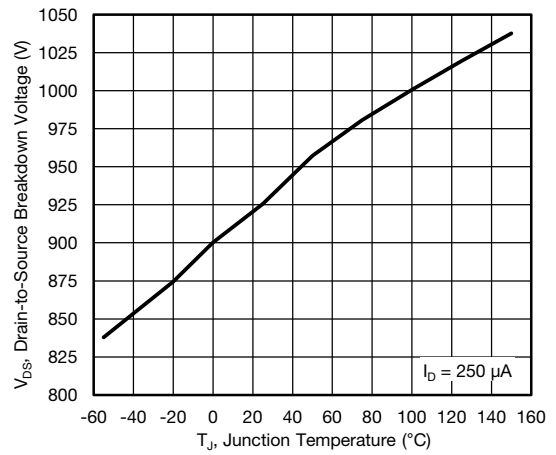


Fig. 11 - Temperature vs. Drain-to-Source Voltage

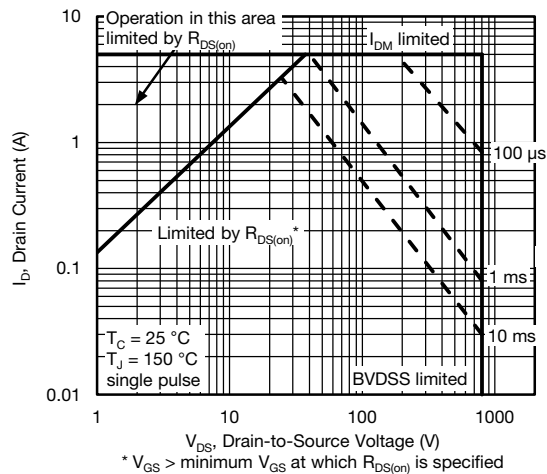
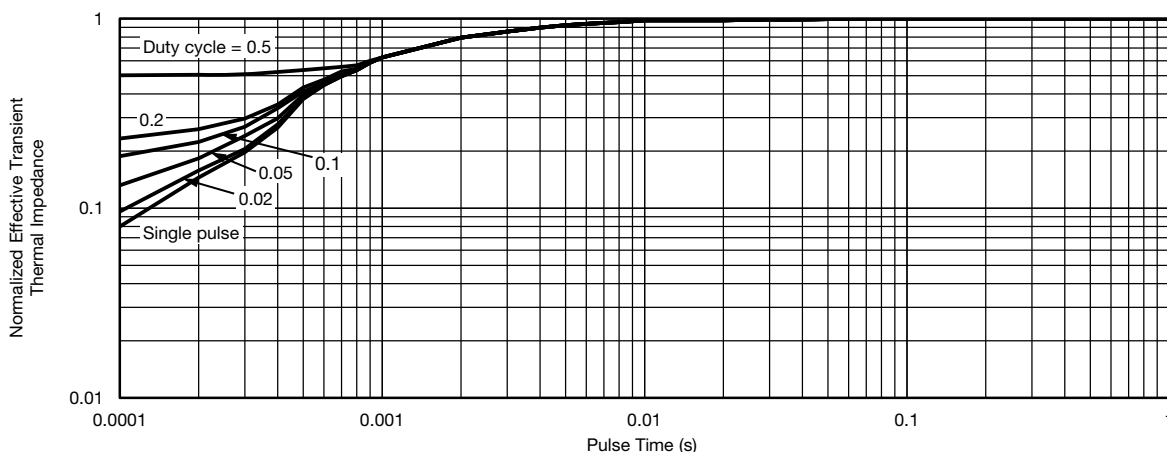
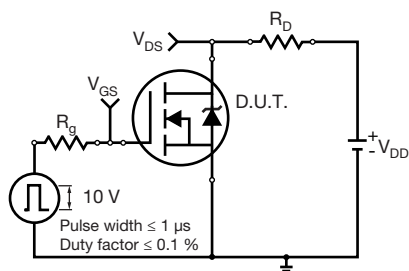


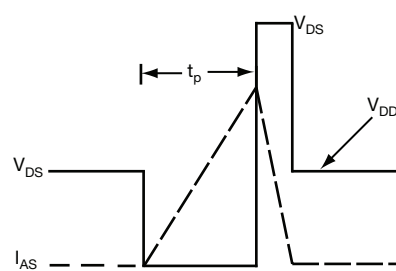
Fig. 9 - Maximum Safe Operating Area



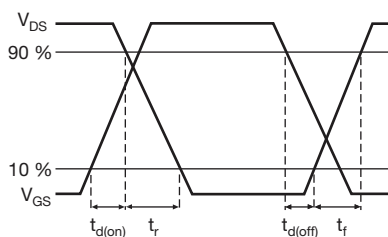
**Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case**



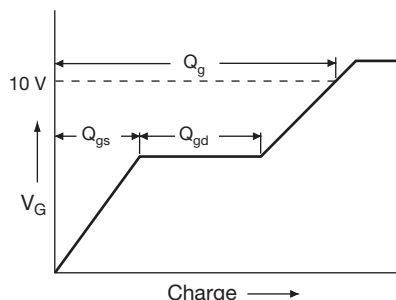
**Fig. 13 - Switching Time Test Circuit**



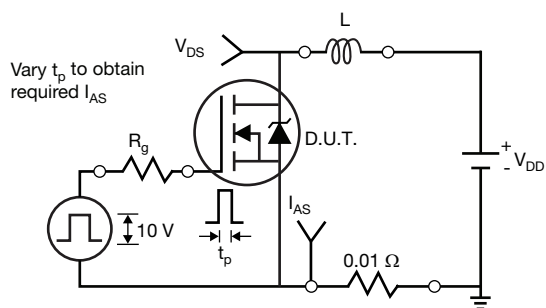
**Fig. 16 - Unclamped Inductive Waveforms**



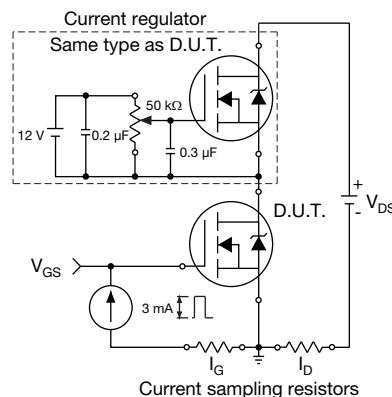
**Fig. 14 - Switching Time Waveforms**



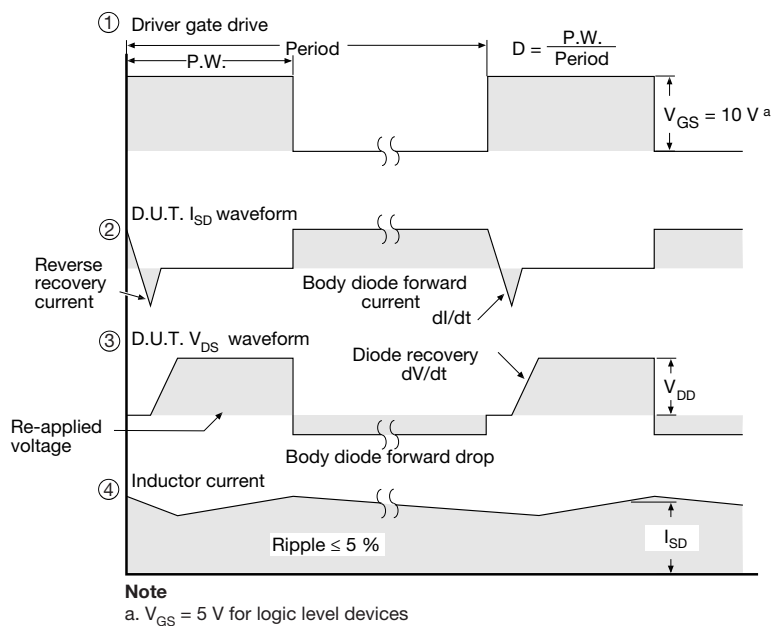
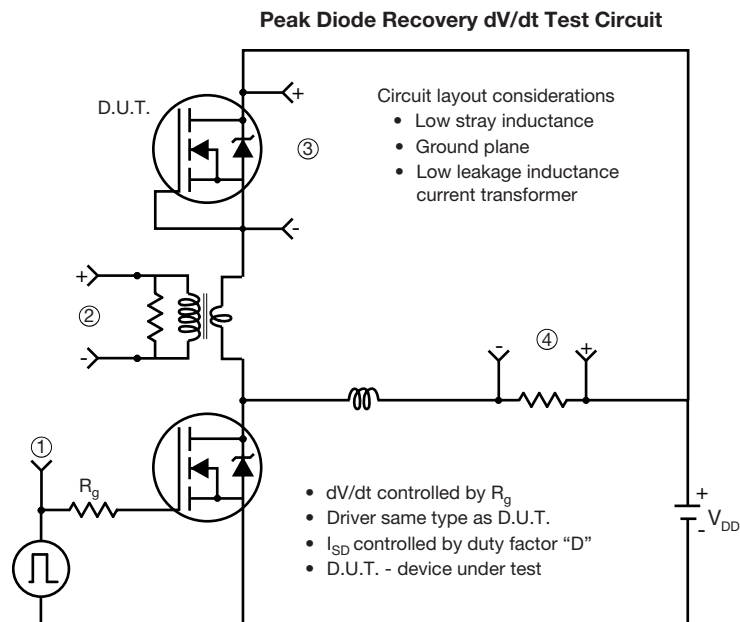
**Fig. 17 - Basic Gate Charge Waveform**



**Fig. 15 - Unclamped Inductive Test Circuit**



**Fig. 18 - Gate Charge Test Circuit**



**Fig. 19 - For N-Channel**

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