

# SVD3410D-VB Datasheet N-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A)			
100	0.114 at V <sub>GS</sub> = 10 V	15			

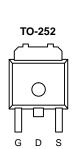
#### **FEATURES**

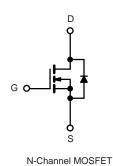
- Trench Power MOSFET
- 150 °C Junction Temperature
- PWM Optimized
- 100 % R<sub>a</sub> Tested
- Compliant to RoHS Directive 2002/95/EC



#### **APPLICATIONS**

· Primary Side Switch





<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>A</sub> = 25 °C, unless otherwise noted)						
Parameter		Symbol	Limit	Unit		
Drain-Source Voltage		V <sub>DS</sub>	100	V		
Gate-Source Voltage		V <sub>GS</sub>	± 20			
Continuous Drain Current (T,I = 175 °C) <sup>b</sup>	T <sub>C</sub> = 25 °C	I <sub>D</sub>	15			
Continuous Drain Current (1, = 175 °C)	T <sub>C</sub> = 125 °C	D D	13			
Pulsed Drain Current		I <sub>DM</sub>	40	A		
Continuous Source Current (Diode Conduction)		I <sub>S</sub>	3			
Avalanche Current	I <sub>AS</sub>	3				
Single Pulse Avalanche Energy	L = 0.1 mH	E <sub>AS</sub>	18	mJ		
Maximum Pawar Dissination	T <sub>C</sub> = 25 °C	P <sub>D</sub>	96 <sup>b</sup>	W		
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	'D	3 <sup>a</sup>	] VV		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
hungation to Ambiens	t ≤ 10 s	- R <sub>thJA</sub>	15	18	°C/W	
Junction-to-Ambient <sup>a</sup>	Steady State		40	50		
Junction-to-Case (Drain)	•	R <sub>thJC</sub>	0.85	1.1		

#### Notes:

- a. Surface mounted on 1" x 1" FR4 board.
- b. See SOA curve for voltage derating.

服务热线:400-655-8788

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Parameter	Symbol	Test Conditions	Min.	Typ. <sup>a</sup>	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	100		V		
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.0		3.5	V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
		V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V		1		
Zero Gate Voltage Drain Current	$I_{DSS}$	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			50	μΑ	
		V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C			250		
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	40			Α	
		$V_{GS} = 10 \text{ V}, I_D = 3 \text{ A}$		0.114			
Danie Course On Chata Besistance	R	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3 A, T <sub>J</sub> = 125 °C		0.120			
Drain-Source On-State Resistance <sup>D</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3 A, T <sub>J</sub> = 175 °C		0.140		Ω	
		$V_{GS} = 4.5 \text{ V } I_D = 3 \text{ A}$		0.120			
Forward Transconductance <sup>b</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 3 A		35		S	
Dynamic <sup>a</sup>							
Input Capacitance	C <sub>iss</sub>			950		pF	
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 \text{ V}, V_{DS} = 25 \text{ V}, F = 1 \text{ MHz}$		120			
Reverse Transfer Capacitance	C <sub>rss</sub>			60			
Total Gate Charge <sup>c</sup>	$Q_g$			24	41		
Gate-Source Charge <sup>c</sup>	$Q_{gs}$	$V_{DS} = 50 \text{ V},  V_{GS} = 10 \text{ V}, I_D = 3 \text{ A}$		8		nC	
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			12			
Gate Resistance	$R_g$		0.5		2.9	Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			15	25		
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = 50 \text{ V}, R_{L} = 5.2 \Omega$		50	75	ns	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	$I_D \cong 3 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 2.5 \Omega$		30	45		
Fall Time <sup>c</sup>	t <sub>f</sub>			60	90		
Source-Drain Diode Ratings and Char	acteristics (7	<sub>C</sub> = 25 °C)					
Pulsed Current	I <sub>SM</sub>				5	Α	
Diode Forward Voltage <sup>b</sup>	$V_{SD}$	I <sub>F</sub> = 3 A, V <sub>GS</sub> = 0 V		0.9	1.5	V	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 3 A, dI/dt = 100 A/µs		180	250	ns	

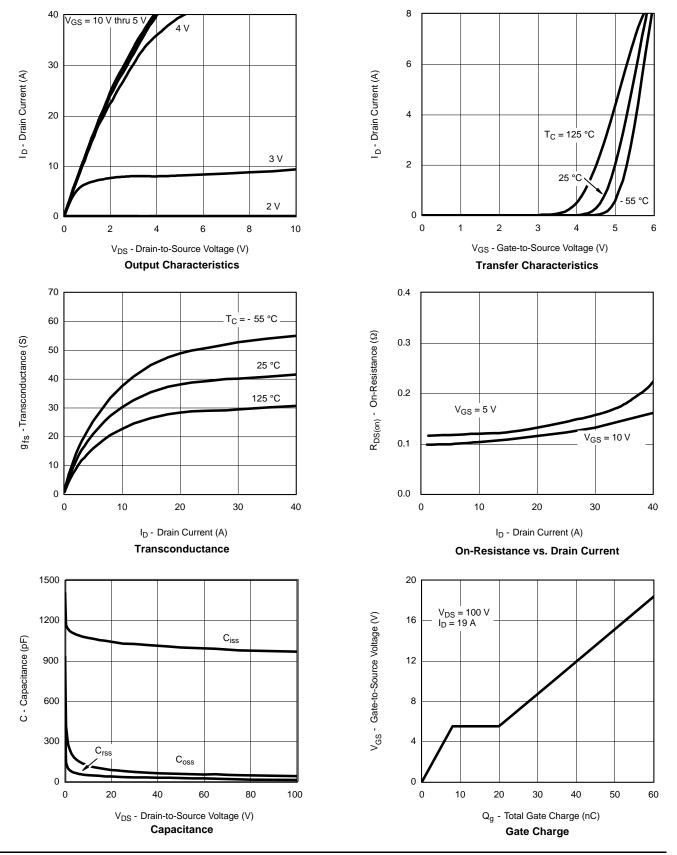
#### Notes:

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

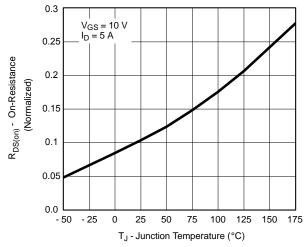


#### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

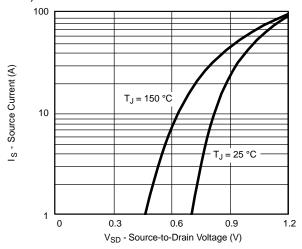




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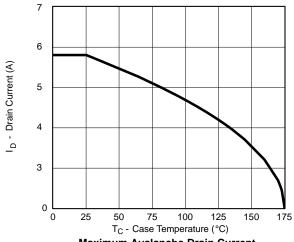


On-Resistance vs. Junction Temperature

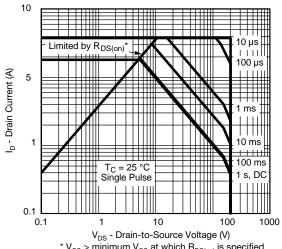


Source-Drain Diode Forward Voltage

#### THERMAL RATINGS

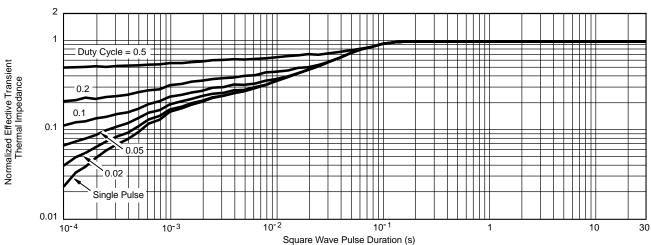


Maximum Avalanche Drain Current vs. Case Temperature



\* V<sub>GS</sub> > minimum V<sub>GS</sub> at which R<sub>DS(on)</sub> is specified

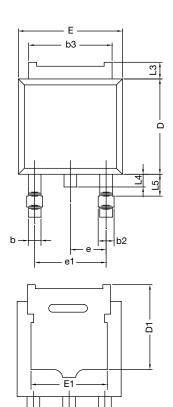
Safe Operating Area

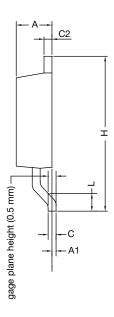


Normalized Thermal Transient Impedance, Junction-to-Case



## **TO-252AA CASE OUTLINE**





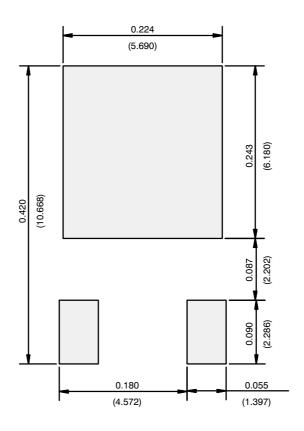
	MILLIMETERS		INCHES		
DIM.	MIN.	MAX.	MIN.	MAX.	
Α	2.18	2.38	0.086	0.094	
A1	-	0.127	-	0.005	
b	0.64	0.88	0.025	0.035	
b2	0.76	1.14	0.030	0.045	
b3	4.95	5.46	0.195	0.215	
С	0.46	0.61	0.018	0.024	
C2	0.46	0.89	0.018	0.035	
D	5.97	6.22	0.235	0.245	
D1	5.21	=	0.205	-	
Е	6.35	6.73	0.250	0.265	
E1	4.32	=	0.170	-	
Н	9.40	10.41	0.370	0.410	
е	2.28 BSC		0.090	BSC	
e1	4.56	BSC	0.180 BSC		
L	1.40	1.78	0.055	0.070	
L3	0.89	1.27	0.035	0.050	
L4	-	1.02	-	0.040	
L5	1.14	1.52	0.045	0.060	
ECN: X12-0247-Rev. M, 24-Dec-12 DWG: 5347					

#### Note

• Dimension L3 is for reference only.



#### **RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)**



Recommended Minimum Pads Dimensions in Inches/(mm)



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