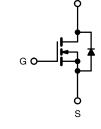


SSR2N80A-VB Datasheet N-Channel 800V (D-S) Super Junction Power MOSFET

PRODUCT SUMMARY						
V_{DS} (V) at T_{J} max.	800					
R _{DS(on)} typ. (Ω) at 25 °C	$V_{GS} = 10 V$	2.38				
Q _g max. (nC)	90					
Q _{gs} (nC)	11					
Q _{gd} (nC)	19					
Configuration	Single					

DPAK (TO-252)



N-Channel MOSFET

FEATURES

- Low figure-of-merit (FOM) Ron x Qg
- Low input capacitance (Ciss)
- · Reduced switching and conduction losses
- Ultra low gate charge (Q_q)
- Avalanche energy rated (UIS)

APPLICATIONS

- · Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
- Renewable energy
- Solar (PV inverters)

ABSOLUTE MAXIMUM RATINGS ($T_c = 25 \text{ °C}$, unless otherwise noted)									
PARAMETER			SYMBOL	LIMIT	UNIT				
Drain-source voltage			V _{DS}	800	V				
Gate-source voltage			V _{GS}	± 30	v				
Continuous drain current (T _J = 150 °C)	V _{GS} at 10 V	$T_{\rm C} = 25 \ ^{\circ}{\rm C}$ $T_{\rm C} = 100 \ ^{\circ}{\rm C}$	- I _D	2.8					
		T _C = 100 °C		1.8	А				
Pulsed drain current ^a			I _{DM}	5					
Linear derating factor				0.5	W/°C				
Single pulse avalanche energy ^b			E _{AS}	14	mJ				
Maximum power dissipation			P _D	62.5	W				
Operating junction and storage temperature range			T _J , T _{stg}	-55 to +150	°C				
Drain-source voltage slope	T _J = 125 °C		a\\//at	70					
Reverse diode dV/dt ^d			dV/dt	0.13	V/ns				
Soldering recommendations (peak temperature) ^c	For	10 s		300	°C				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature

- b. V_{DD} = 140 V, starting T_J = 25 °C, L = 28.2 mH, R_g = 25 $\Omega,\,I_{AS}$ = 0.9 A
- c. 1.6 mm from case
- d. $I_{SD} \leq I_D$, dl/dt = 100 A/µs, starting T_J = 25 °C



HALOGEN

FREE



THERMAL RESISTANCE RAT	NGS								
PARAMETER	SYMBOL	TYP.		MAX.		UNIT			
Maximum junction-to-ambient	R _{thJA}	- 62							
Maximum junction-to-case (drain)	R _{thJC}	- 2.0				°C/W			
SPECIFICATIONS (T _J = 25 °C, u	unless otherwi	se noted)							
PARAMETER	SYMBOL	TES	T CONDIT	IONS	MIN.	TYP.	MAX.	UNIT	
Static	•					•			
Drain-source breakdown voltage	V _{DS}	V _{GS} =	0 V, I _D = 2	250 µA	800	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference	e to 25 °C,	$I_D = 1 \text{ mA}$	-	1.0	-	V/°C	
Gate-source threshold Voltage (N)	V _{GS(th)}	V _{DS} =	$= V_{GS}, I_D =$	250 µA	2.0	-	4.0	V	
Gate-source leakage	I _{GSS}	$V_{GS} = \pm 20 \text{ V}$			-	-	± 100	nA	
			$V_{GS} = \pm 30 \text{ V}$			-	± 1	μA	
		V _{DS} =	V _{DS} = 800 V, V _{GS} = 0 V			-	1	μA	
Zero gate voltage drain current	IDSS	$V_{DS} = 640 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 125 \text{ °C}$			-	-	10		
Drain-source on-state resistance	R _{DS(on)}	$V_{GS} = 10 V$	I	_D = 1.0 A	-	2.38	-	Ω	
Forward transconductance	9 _{fs}	V _{DS}	= 30 V, I _D =	= 1.0 A	-	1.0	-	S	
Dynamic	•					•			
Input capacitance	C _{iss}		$V_{GS} = 0 V$	1	-	315	-		
Output capacitance	C _{oss}	$V_{DS} = 100 V,$		-	20	-	1		
Reverse transfer capacitance	C _{rss}		$\overline{f} = 1 \text{ MHz}$		-	6	-		
Effective output capacitance, energy related ^a	C _{o(er)}	$V_{DS} = 0 V$ to 480 V, $V_{GS} = 0 V$		-	13	-	pF		
Effective output capacitance, time related ^b	C _{o(tr)}			-	45	-			
Total gate charge	Qg				-	9.8	19.6		
Gate-source charge	Q _{gs}	V _{GS} = 10 V I _D = 1.0 A, V _{DS} = 480 V		-	2.4	-	nC		
Gate-drain charge	Q _{gd}				-	3.9	-		
Turn-on delay time	t _{d(on)}	V _{DD} = 480 V, I _D = 1.0 A,		-	11	22			
Rise time	t _r			-	7	14			
Turn-off delay time	t _{d(off)}		$V_{\rm GS} = 400$ V, $R_{\rm g} = 1.0$ A, $V_{\rm GS} = 10$ V, $R_{\rm g} = 9.1$ Ω		-	19	38	ns	
Fall time	t _f	f = 1 MHz, open drain		-	27	54			
Gate input resistance	R _g			1.8	3.6	7.2	Ω		
Drain-Source Body Diode Characteristi	cs								
Continuous source-drain diode current	١ _S	MOSFET sym showing the	MOSFET symbol showing the		-	-	2.8		
Pulsed diode forward current	I _{SM}	integral reverse p - n junction diode		-	-	5	A		
Diode forward voltage	V _{SD}	T _J = 25 °C, I _S = 11 A, V _{GS} = 0 V		-	-	1.2	V		
Reverse recovery time	t _{rr}				-	278	556	ns	
Reverse recovery charge	Q _{rr}	$T_J = 25 \text{ °C}, I_F = I_S = 1.0 \text{ A},$ dl/dt = 100 A/µs, V _R = 25 V		-	0.9	1.8	μC		
Reverse recovery current	I _{RRM}			-	5	-	A		

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

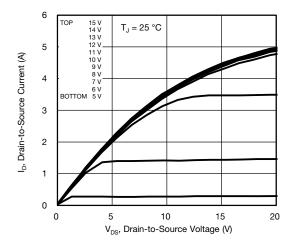
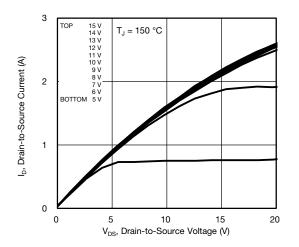


Fig. 1 - Typical Output Characteristics





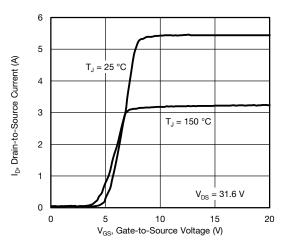


Fig. 3 - Typical Transfer Characteristics

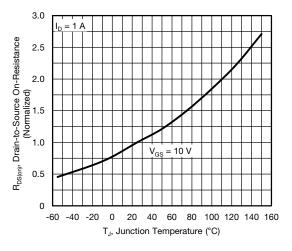


Fig. 4 - Normalized On-Resistance vs. Temperature

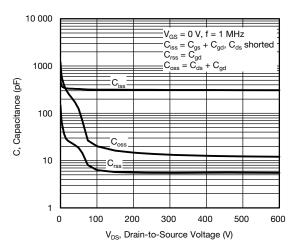


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

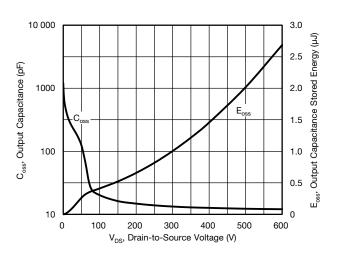


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

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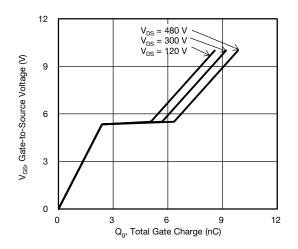


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

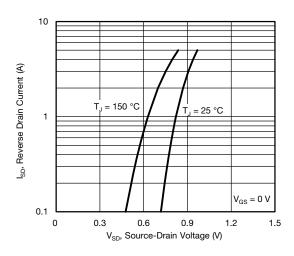


Fig. 8 - Typical Source-Drain Diode Forward Voltage

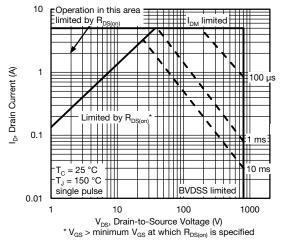


Fig. 9 - Maximum Safe Operating Area

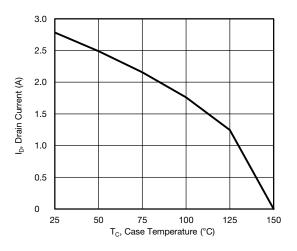


Fig. 10 - Maximum Drain Current vs. Case Temperature

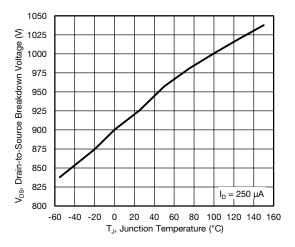
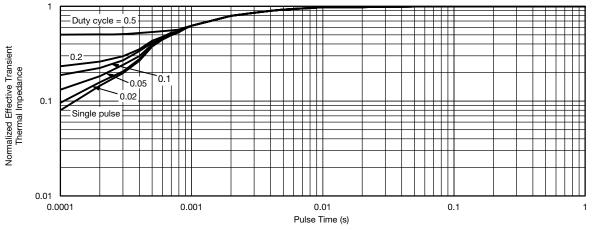


Fig. 11 - Temperature vs. Drain-to-Source Voltage

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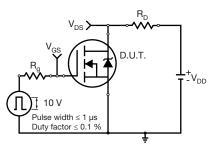


Fig. 13 - Switching Time Test Circuit

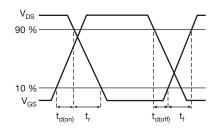


Fig. 14 - Switching Time Waveforms

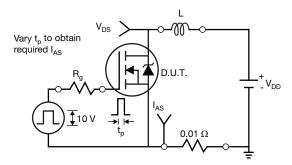


Fig. 15 - Unclamped Inductive Test Circuit

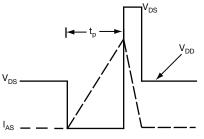


Fig. 16 - Unclamped Inductive Waveforms

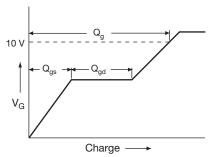


Fig. 17 - Basic Gate Charge Waveform

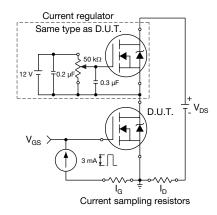


Fig. 18 - Gate Charge Test Circuit

semi

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Peak Diode Recovery dV/dt Test Circuit

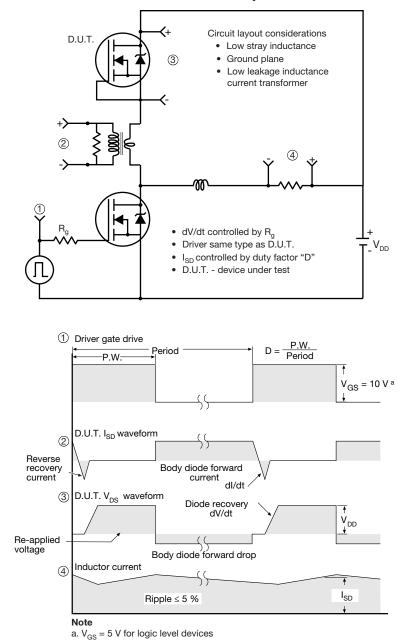


Fig. 19 - For N-Channel



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