

SM2F04NSU-VB Datasheet

N-Channel 250 V (D-S) 175 °C MOSFET

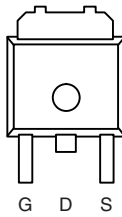
| PRODUCT SUMMARY | | |
|---------------------------|------------------------|-------|
| V_{DS} (V) | 250 | |
| $R_{DS(on)}$ (Ω) | $V_{GS} = 10\text{ V}$ | 0.176 |
| Q_g max. (nC) | 68 | |
| Q_{gs} (nC) | 11 | |
| Q_{gd} (nC) | 35 | |
| Configuration | Single | |

FEATURES

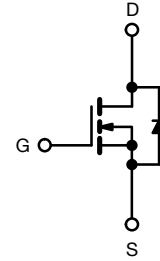
- Dynamic dV/dt rating
- Repetitive avalanche rated
- Fast switching
- Ease of paralleling
- Simple drive requirements



TO-252



Top View



N-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted) | | | | | | |
|---|-------------------------|-------------------------|-----------------------------------|----------------|----------|---|
| PARAMETER | | | SYMBOL | LIMIT | UNIT | |
| Drain-Source Voltage | | | V _{DS} | 250 | V | |
| Gate-Source Voltage | | | V _{GS} | ± 20 | | |
| Continuous Drain Current | V _{GS} at 10 V | T _C = 25 °C | I _D | 17 | A | |
| | | T _C = 100 °C | | 11 | | |
| Pulsed Drain Current ^a | | | I _{DM} | 56 | | |
| Linear Derating Factor | | | | 1.0 | W/°C | |
| Single Pulse Avalanche Energy ^b | | | E _{AS} | 550 | mJ | |
| Repetitive Avalanche Current ^a | | | I _{AR} | 17 | A | |
| Repetitive Avalanche Energy ^a | | | E _{AR} | 13 | mJ | |
| Maximum Power Dissipation | | T _C = 25 °C | | P _D | 125 | W |
| Peak Diode Recovery dV/dt ^c | | | dV/dt | 4.8 | V/ns | |
| Operating Junction and Storage Temperature Range | | | T _J , T _{stg} | -55 to +150 | °C | |
| Soldering Recommendations (Peak temperature) ^d | | for 10 s | | 300 | | |
| Mounting Torque | 6-32 or M3 screw | | | 10 | lbf · in | |
| | | | | 1.1 | N · m | |

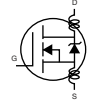

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{PD} = 50\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 4.5\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 14\text{ A}$ (see fig. 12).
- $I_{SD} \leq 14\text{ A}$, $dI/dt \leq 150\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.

THERMAL RESISTANCE RATINGS

| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
|-------------------------------------|------------|------|------|------|
| Maximum Junction-to-Ambient | R_{thJA} | - | 62 | °C/W |
| Case-to-Sink, Flat, Greased Surface | R_{thCS} | 0.50 | - | |
| Maximum Junction-to-Case (Drain) | R_{thJC} | - | 1.0 | |

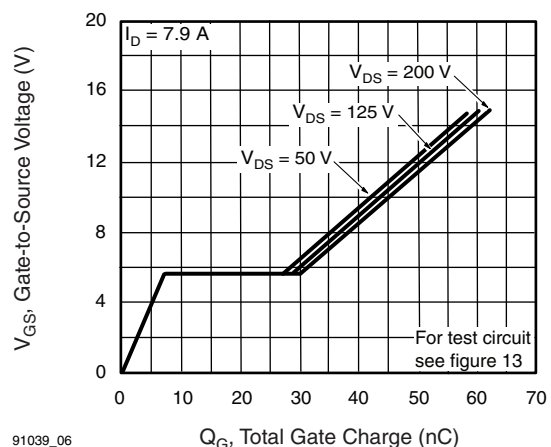
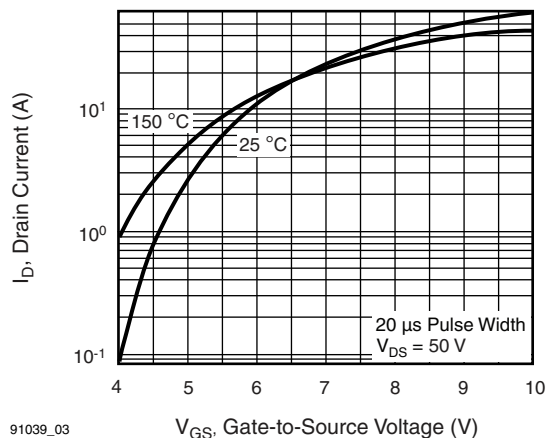
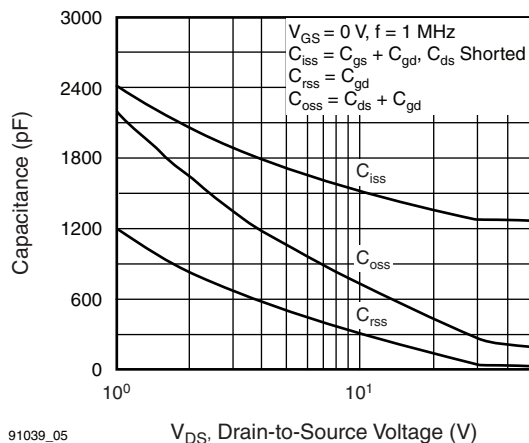
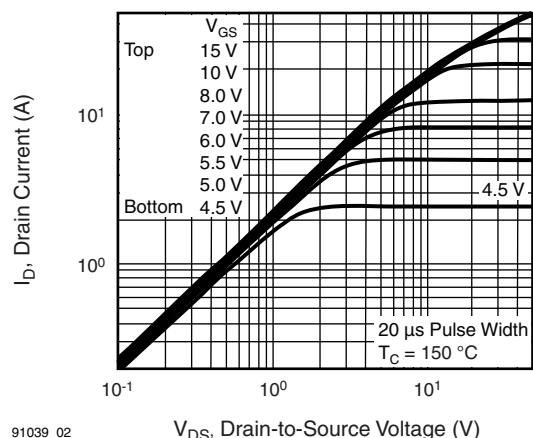
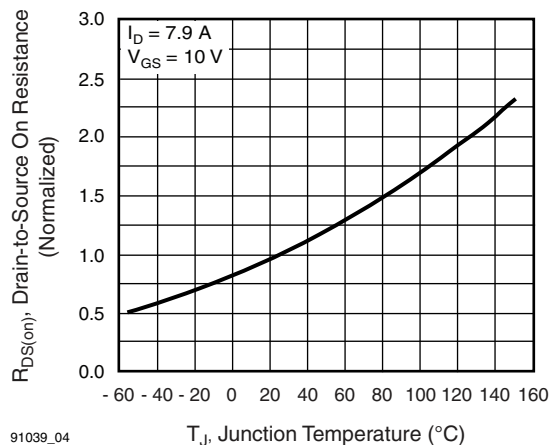
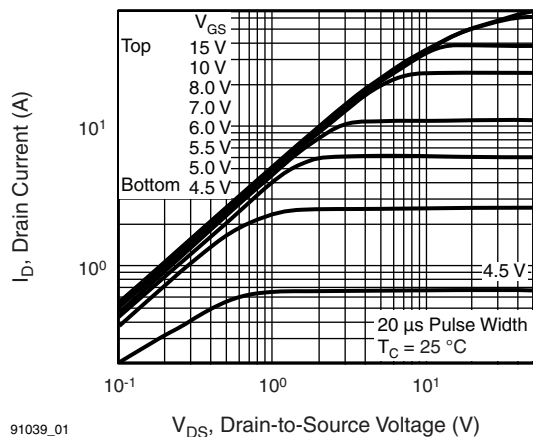
SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|---------------------|---|------|-------|-----------|-----------------------|
| Static | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$ | 250 | - | - | V |
| V_{DS} Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to $25\text{ }^{\circ}\text{C}$, $I_D = 1\text{ mA}$ | - | 0.34 | - | V/ $^{\circ}\text{C}$ |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$ | 2.0 | - | 4.0 | V |
| Gate-Source Leakage | I_{GSS} | $V_{GS} = \pm 20\text{ V}$ | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 250\text{ V}$, $V_{GS} = 0\text{ V}$ | - | - | 25 | μA |
| | | $V_{DS} = 200\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$ | - | - | 250 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$, $I_D = 8.4\text{ A}^b$ | - | 0.176 | - | Ω |
| Forward Transconductance | g_{fs} | $V_{DS} = 50\text{ V}$, $I_D = 8.4\text{ A}^b$ | 6.7 | - | - | S |
| Dynamic | | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5 | - | 1300 | - | pF |
| Output Capacitance | C_{oss} | | - | 330 | - | |
| Reverse Transfer Capacitance | C_{rss} | | - | 85 | - | |
| Total Gate Charge | Q_g | $V_{GS} = 10\text{ V}$, $I_D = 7.9\text{ A}$, $V_{DS} = 200\text{ V}$, see fig. 6 and 13 ^b | - | - | 68 | nC |
| Gate-Source Charge | Q_{gs} | | - | - | 11 | |
| Gate-Drain Charge | Q_{gd} | | - | - | 35 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 125\text{ V}$, $I_D = 7.9\text{ A}$, $R_g = 9.1\text{ }\Omega$, $R_D = 8.7\text{ }\Omega$, see fig. 10 ^b | - | 11 | - | ns |
| Rise Time | t_r | | - | 24 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 53 | - | |
| Fall Time | t_f | | - | 49 | - | |
| Internal Drain Inductance | L_D | Between lead, 6 mm (0.25") from package and center of die contact  | - | 4.5 | - | nH |
| Internal Source Inductance | L_S | | - | 7.5 | - | |
| Gate Input Resistance | R_g | $f = 1\text{ MHz}$, open drain | 0.3 | - | 1.2 | Ω |
| Drain-Source Body Diode Characteristics | | | | | | |
| Continuous Source-Drain Diode Current | I_S | MOSFET symbol showing the integral reverse p - n junction diode  | - | - | 14 | A |
| Pulsed Diode Forward Current ^a | I_{SM} | | - | - | 56 | |
| Body Diode Voltage | V_{SD} | $T_J = 25\text{ }^{\circ}\text{C}$, $I_S = 14\text{ A}$, $V_{GS} = 0\text{ V}^b$ | - | - | 1.8 | V |
| Body Diode Reverse Recovery Time | t_{rr} | $T_J = 25\text{ }^{\circ}\text{C}$, $I_F = 7.9\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}^b$ | - | 250 | 500 | ns |
| Body Diode Reverse Recovery Charge | Q_{rr} | | - | 2.3 | 4.6 | μC |
| Forward Turn-On Time | t_{on} | Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D) | | | | |

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
 b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



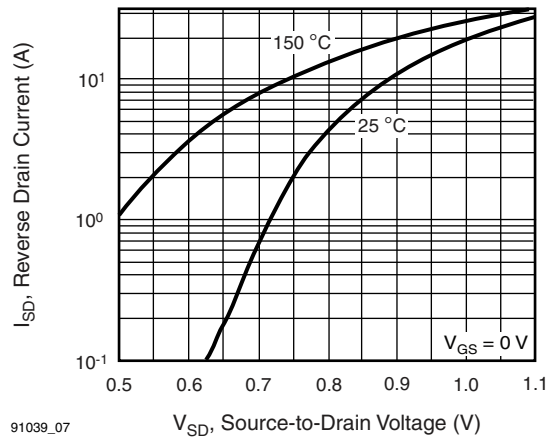


Fig. 7 - Typical Source-Drain Diode Forward Voltage

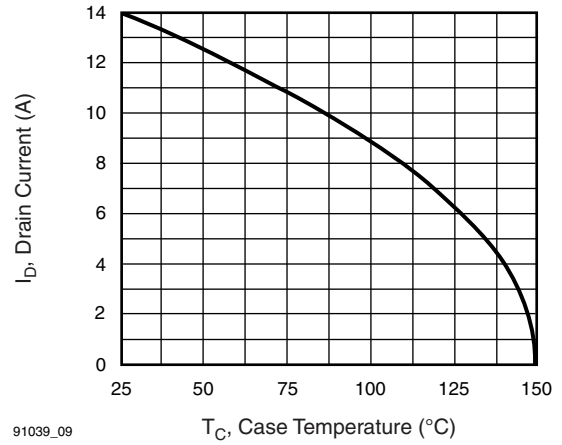


Fig. 9 - Maximum Drain Current vs. Case Temperature

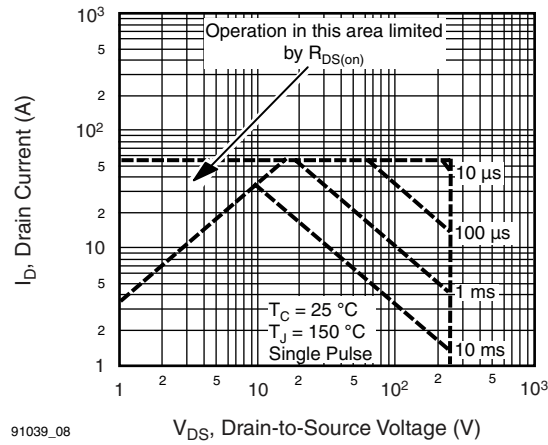


Fig. 8 - Maximum Safe Operating Area

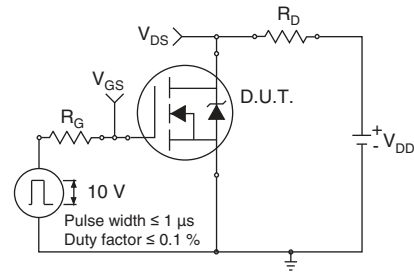


Fig. 10a - Switching Time Test Circuit

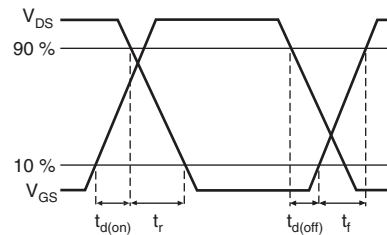


Fig. 10b - Switching Time Waveforms

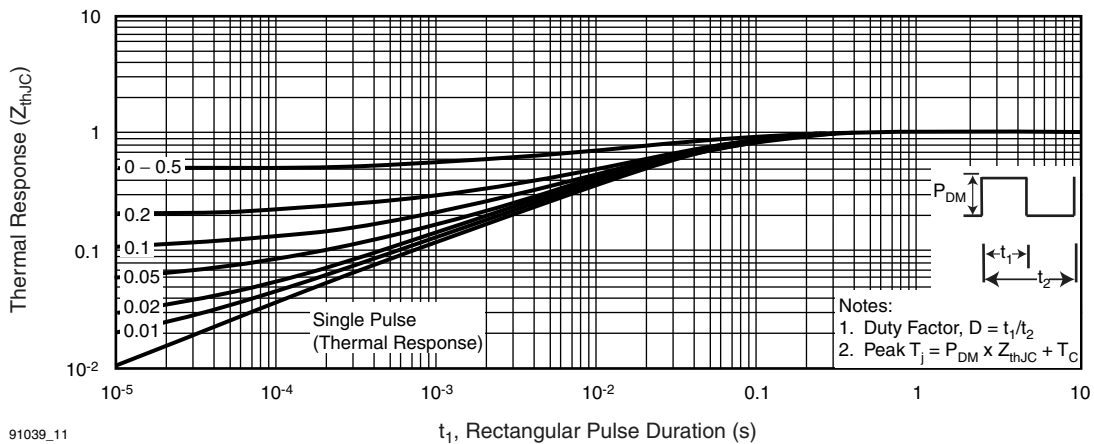


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

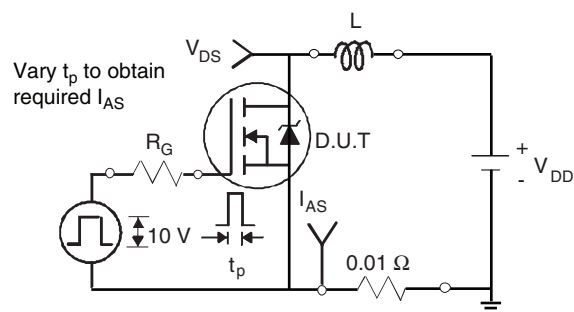


Fig. 12a - Unclamped Inductive Test Circuit

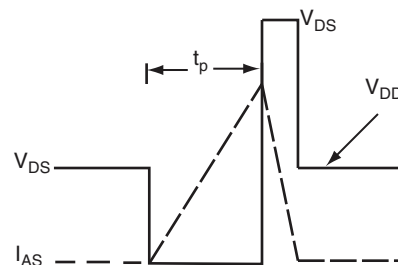


Fig. 12b - Unclamped Inductive Waveforms

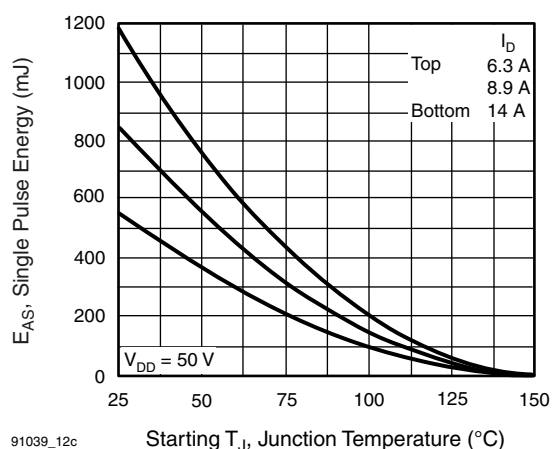


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

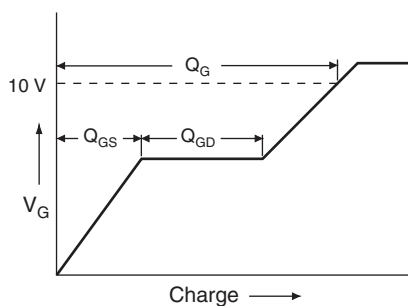


Fig. 13a - Basic Gate Charge Waveform

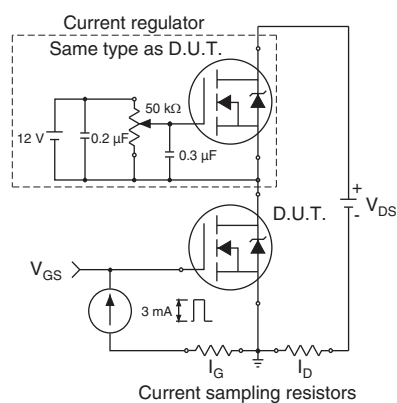
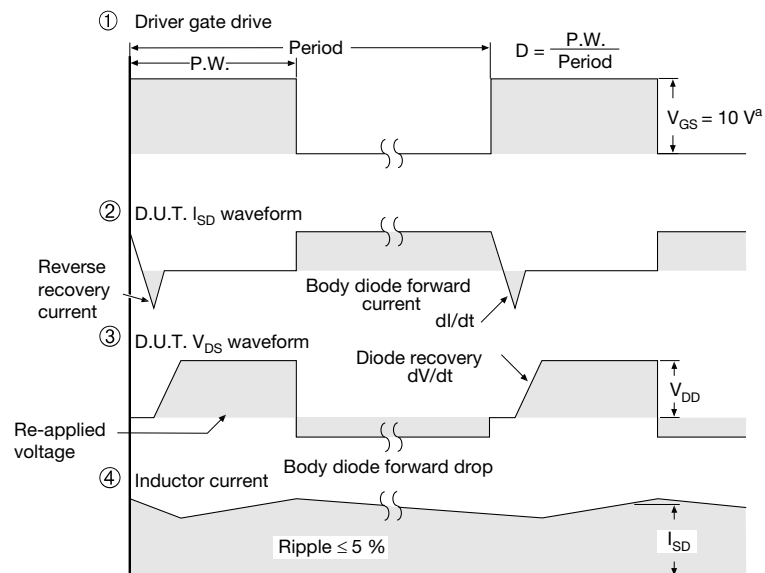
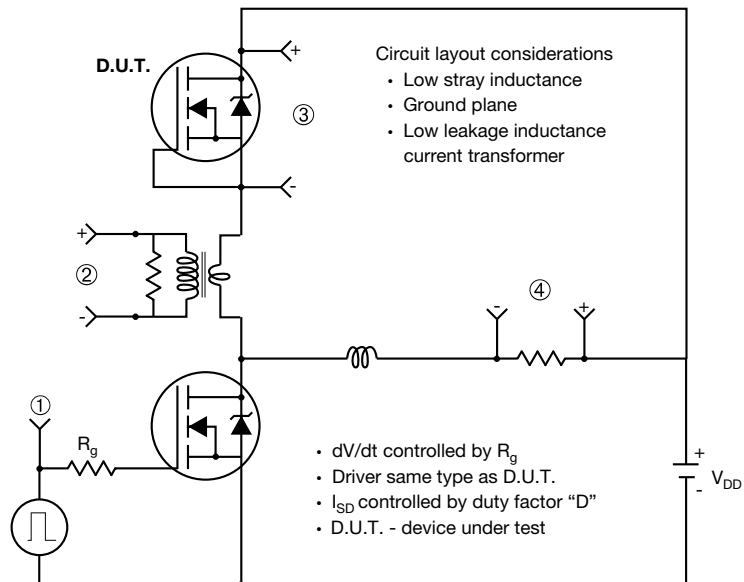


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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