

PHD16N03T-VB Datasheet

N-Channel 30-V (D-S) MOSFET

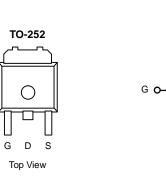
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- Trench Power MOSFET •
- ٠ •
- 100 % R_g and UIS Tested Compliant to RoHS Directive 2011/65/EU

APPLICATIONS

- OR-ing
- Server
- DC/DC

PRODUCT SUMMARY							
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^{a, e}	Q _g (Typ)				
30	0.007 at V _{GS} = 10 V	70	25 nC				
30	0.009 at V _{GS} = 4.5 V	60	23110				



S

D

N-Channel MOSFET

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	30	V	
Gate-Source Voltage		V _{GS}	± 20	V	
	T _C = 25 °C		70	A	
Continuous Drain Current (T _{.1} = 175 °C)	T _C = 70 °C		50		
Continuous Drain Current $(1_j = 175^{\circ} C)$	T _A = 25 °C	I _D	21.8 ^{b, c}		
	T _A = 70 °C		18 ^{b, c}		
Pulsed Drain Current		I _{DM}	200		
Avalanche Current Pulse	L = 0.1 mH	I _{AS}	39		
Single Pulse Avalanche Energy	L = 0.1 MH	E _{AS}	94.8	mJ	
Continuous Source-Drain Diode Current	T _C = 25 °C	L.	50 ^{a, e}	A	
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	3.13 ^{b, c}		
	T _C = 25 °C		100 ^a	w	
	T _C = 70 °C	PD	75		
Maximum Power Dissipation	T _A = 25 °C	r _D	3.25 ^{b, c}		
	T _A = 70 °C		2.33 ^{b, c}		
Operating Junction and Storage Temperature Ra	ange	T _J , T _{stg}	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Тур.	Max.	Unit		
Maximum Junction-to-Ambient ^{b, d}	$t \le 10 \text{ sec}$	R _{thJA}	32	40	°C/W		
Maximum Junction-to-Case	Steady State	R _{thJC}	0.5	0.6	0/10		

Notes:

a. Based on $T_C = 25 \text{ °C}$. b. Surface mounted on 1" x 1" FR4 board.

c. t = 10 sec.
d. Maximum under steady state conditions is 90 °C/W.
e. Calculated based on maximum junction temperature. Package limitation current is 90 A.



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static	- 1					
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 V, I_{D} = 250 \mu A$	30			V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	L _ 250 uA		35		
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA		- 7.5		mV/°C
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \ \mu A$	1.5		2.0	V
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA
		$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			1	
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 55 \text{ °C}$			10	μA
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, \text{ V}_{GS} = 10 \text{ V}$	90			Α
		V _{GS} = 10 V, I _D = 21.8 A		0.007		Ω
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 18A		0.009		
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 21.8 A		160		S
Dynamic ^b						
Input Capacitance	C _{iss}			2201		
Output Capacitance	C _{oss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz		525		pF
Reverse Transfer Capacitance	C _{rss}			370		
	Qg	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 21.8 A		35	45	nC
Total Gate Charge				25	35	
Gate-Source Charge	Q _{gs}	V_{DS} = 15 V, V_{GS} = 4.5 V, I_{D} = 21.8 A		15		
Gate-Drain Charge	Q _{gd}			20		
Gate Resistance	Rg	f = 1 MHz		1.4	2.1	Ω
Turn-On Delay Time	t _{d(on)}			18	27	
Rise Time	t _r	V_{DD} = 15 V, R _L = 0.625 Ω		11	17	
Turn-Off Delay Time	t _{d(off)}	$\text{I}_{\text{D}}\cong$ 24 A, V_{GEN} = 10 V, R_{g} = 1 Ω		70	105	
Fall Time	t _f			10	15	
Turn-On Delay Time	t _{d(on)}			55	83	ns
Rise Time	t _r	V_{DD} = 15 V, R_L = 0.67 Ω		180	270	
Turn-Off Delay Time	t _{d(off)}	${ m I}_{ m D}\cong$ 22.5 A, ${ m V}_{ m GEN}$ = 4.5 V, ${ m R}_{ m g}$ = 1 Ω		55	83	
Fall Time	t _f			12	18	
Drain-Source Body Diode Characteristic	s					1
Continuous Source-Drain Diode Current	۱ _S	T _C = 25 °C			120	^
Pulse Diode Forward Current ^a	I _{SM}				120	A
Body Diode Voltage	V _{SD}	I _S = 22 A		0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}			52	78	ns
Body Diode Reverse Recovery Charge	Q _{rr}			70.2	105	nC
Reverse Recovery Fall Time	t _a	I _F = 20 A, di/dt = 100 A/μs, T _J = 25 °C		27		
Reverse Recovery Rise Time	t _b	—		25		ns

Notes:

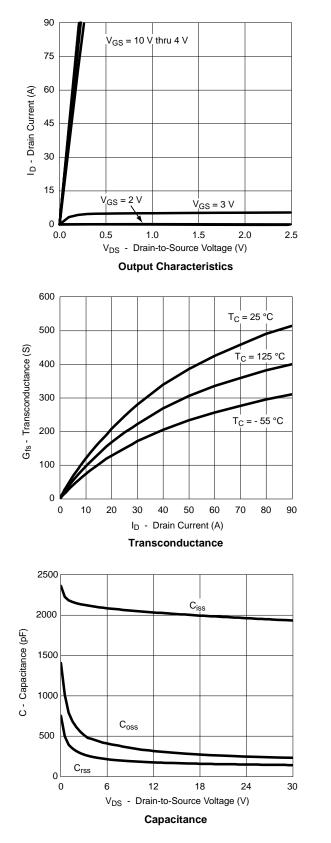
a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle ≤ 2 %.

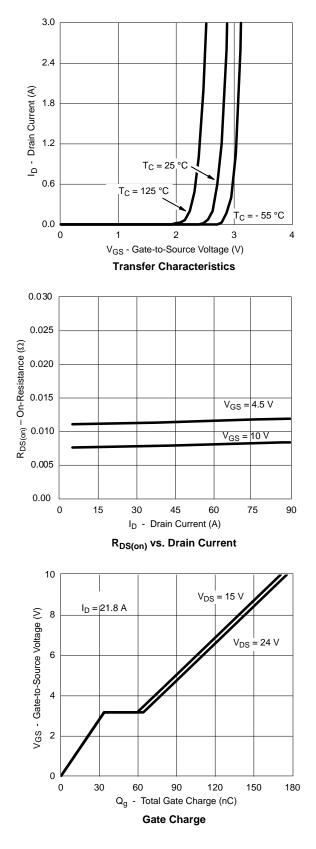
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



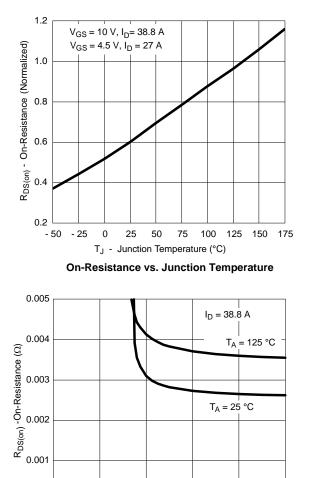


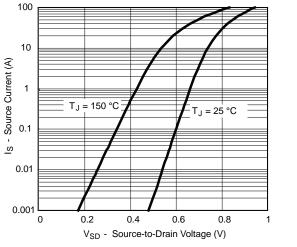




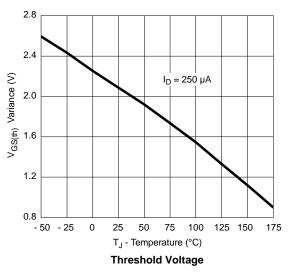


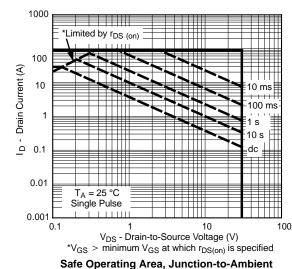
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





Forward Diode Voltage vs. Temperature





0.000

0

2

4

6

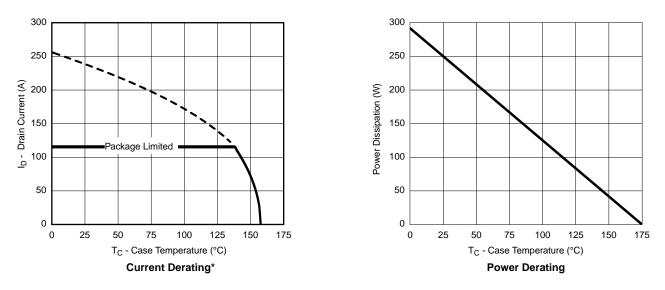
 V_{GS} - Gate-to-Source Voltage (V)

 $R_{DS(on)}$ vs. V_{GS} vs. Temperature

8

10





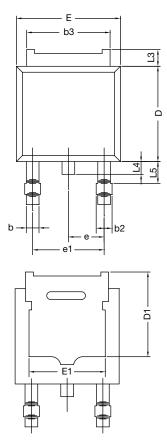
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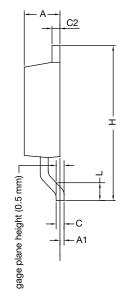
*The power dissipation P_D is based on $T_{J(max)} = 175$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





TO-252AA CASE OUTLINE





	MILLIN	METERS	INCHES				
DIM.	MIN.	MAX.	MIN.	MAX.			
А	2.18	2.38	0.086	0.094			
A1	-	0.127	-	0.005			
b	0.64	0.88	0.025	0.035			
b2	0.76	1.14	0.030	0.045			
b3	4.95	5.46	0.195	0.215			
С	0.46	0.61	0.018	0.024			
C2	0.46	0.89	0.018	0.035			
D	5.97	6.22	0.235	0.245			
D1	5.21	-	0.205	-			
E	6.35	6.73	0.250	0.265			
E1	4.32	-	0.170	-			
Н	9.40	10.41	0.370	0.410			
е	2.28	BSC	0.090 BSC				
e1	4.56 BSC		0.180 BSC				
L	1.40	1.78	0.055	0.070			
L3	0.89	1.27	0.035	0.050			
L4	-	1.02	-	0.040			
L5	1.14	1.52	0.045	0.060			
ECN: X12-0247-Rev. M, 24-Dec-12 DWG: 5347							

Note

• Dimension L3 is for reference only.



RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads Dimensions in Inches/(mm)



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