

## J528STL-E-VB Datasheet

### P-Channel 60-V (D-S) MOSFET

#### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)	$Q_g$ (Typ)
- 60	0.061 at $V_{GS} = - 10$ V	- 30	10
	0.072 at $V_{GS} = - 4.5$ V	- 25	

#### FEATURES

- Trench Power MOSFET
- 100 % UIS Tested

#### APPLICATIONS

- Load Switch



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**



P-Channel MOSFET

#### ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted

Parameter		Symbol	Limit	Unit
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Continuous Drain Current ( $T_J = 175\text{ }^\circ\text{C}$ )	$T_C = 25\text{ }^\circ\text{C}$	$I_D$	- 30	A
	$T_C = 100\text{ }^\circ\text{C}$		- 25	
Pulsed Drain Current		$I_{DM}$	- 30	
Continuing Source Current (Diode Conduction)		$I_S$	- 20	
Avalanche Current		$I_{AS}$	- 20	
Single Pulse Avalanche Energy	$L = 0.1\text{ mH}$	$E_{AS}$	7.2	mJ
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	$P_D$	34 <sup>a</sup>	W
	$T_A = 25\text{ }^\circ\text{C}$		4 <sup>b</sup>	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to 175	$^\circ\text{C}$

#### THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient <sup>b</sup>	$t \leq 10\text{ sec}$	$R_{thJA}$	20	25	$^\circ\text{C/W}$
	Steady State		62	75	
Junction-to-Case		$R_{thJC}$	5	6	

Notes:

a. See SOA curve for voltage derating.

b. Surface Mounted on 1" x 1" FR-4 board.

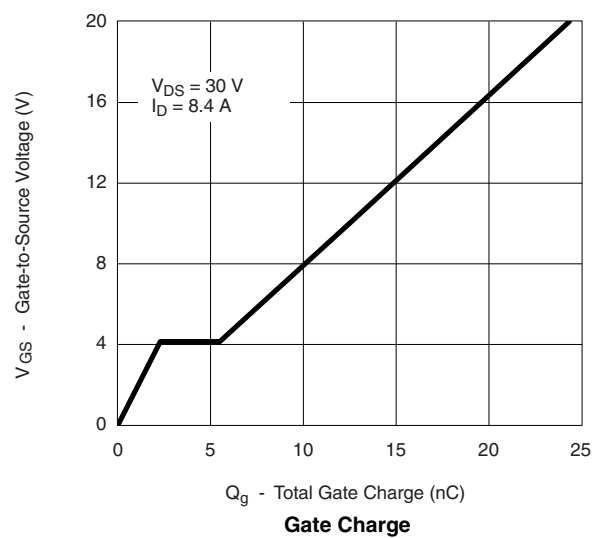
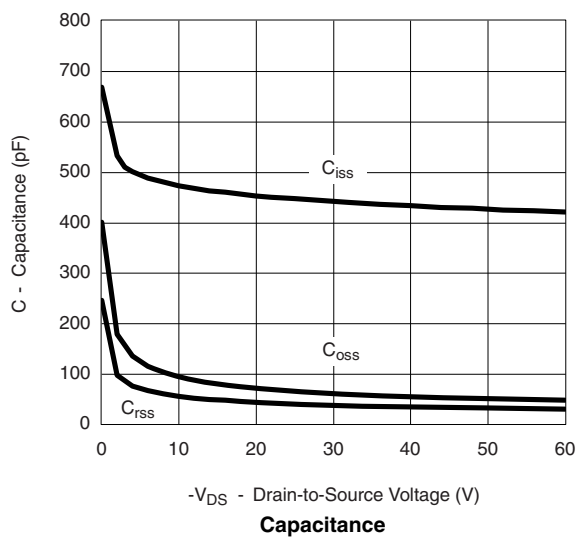
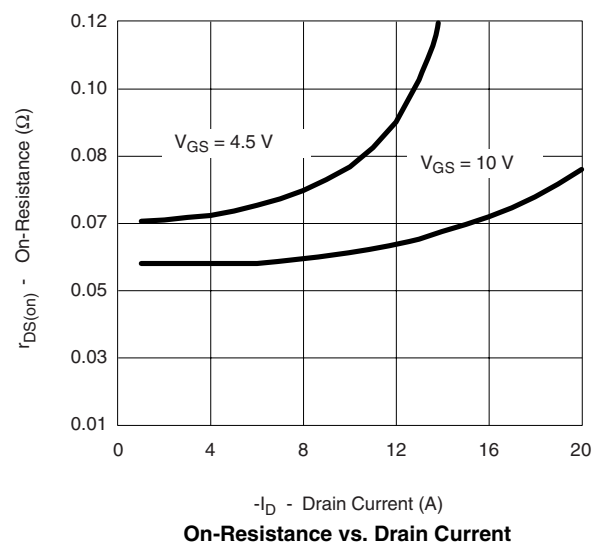
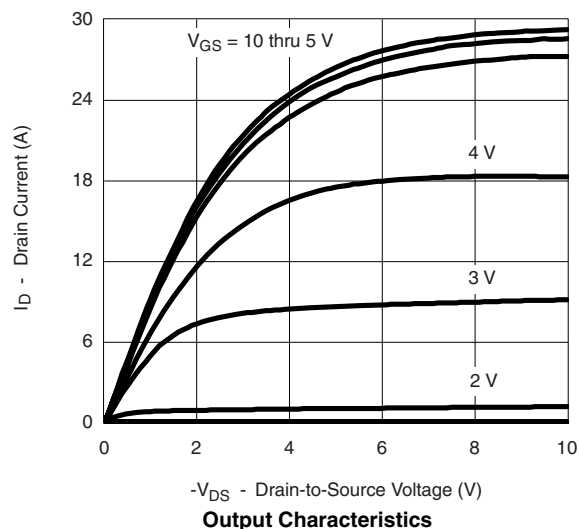
SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min	Typ <sup>a</sup>	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}$ , $I_D = -250\text{ }\mu\text{A}$	- 60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = -250\text{ }\mu\text{A}$	- 1.0	- 2.0	- 3.0	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -60\text{ V}$ , $V_{GS} = 0\text{ V}$			- 1	$\mu\text{A}$
		$V_{DS} = -60\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ }^{\circ}\text{C}$			- 50	
		$V_{DS} = -60\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 175\text{ }^{\circ}\text{C}$			- 150	
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{DS} = -5\text{ V}$ , $V_{GS} = -10\text{ V}$	- 10			A
Drain-Source On-State Resistance <sup>b</sup>	$r_{DS(on)}$	$V_{GS} = -10\text{ V}$ , $I_D = -5\text{ A}$		0.061		$\Omega$
		$V_{GS} = -10\text{ V}$ , $I_D = -5\text{ A}$ , $T_J = 125\text{ }^{\circ}\text{C}$		0.100		
		$V_{GS} = -10\text{ V}$ , $I_D = -5\text{ A}$ , $T_J = 175\text{ }^{\circ}\text{C}$		0.150		
		$V_{GS} = -4.5\text{ V}$ , $I_D = -2\text{ A}$		0.072		
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = -15\text{ V}$ , $I_D = -5\text{ A}$		8		S
Dynamic						
Input Capacitance	$C_{iss}$	$V_{DS} = -25\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		1000		pF
Output Capacitance	$C_{oss}$			120		
Reverse Transfer Capacitance	$C_{rss}$			100		
Total Gate Charge	$Q_g$	$V_{DS} = -30\text{ V}$ , $V_{GS} = -10\text{ V}$ , $I_D = -8.4\text{ A}$		10		nC
Gate-Source Charge	$Q_{gs}$			2.1		
Gate-Drain Charge	$Q_{gd}$			3.2		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$		8.0		$\Omega$
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = -30\text{ V}$ , $R_L = 3.57\text{ }\Omega$ $I_D \cong -8.4\text{ A}$ , $V_{GEN} = -10\text{ V}$ , $R_G = 2.5\text{ }\Omega$		6		ns
Rise Time <sup>c</sup>	$t_r$			15		
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			16		
Fall Time <sup>c</sup>	$t_f$			8		
Source-Drain Diode Ratings and Characteristics ( $T_C = 25\text{ }^{\circ}\text{C}$ ) <sup>b</sup>						
Pulsed Current	$I_{SM}$				- 30	A
Forward Voltage <sup>b</sup>	$V_{SD}$	$I_F = -2\text{ A}$ , $V_{GS} = 0\text{ V}$		- 0.9	- 1.3	V
Reverse Recovery Time	$t_{rr}$	$I_F = -8\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		50		ns
Reverse Recovery Time	$Q_{rr}$			80		nC

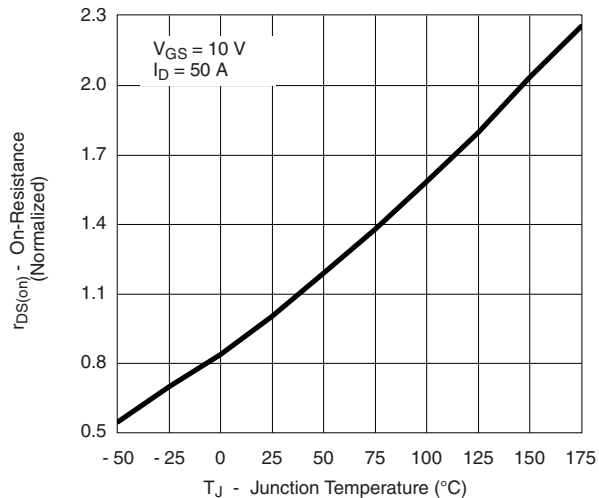
Notes:

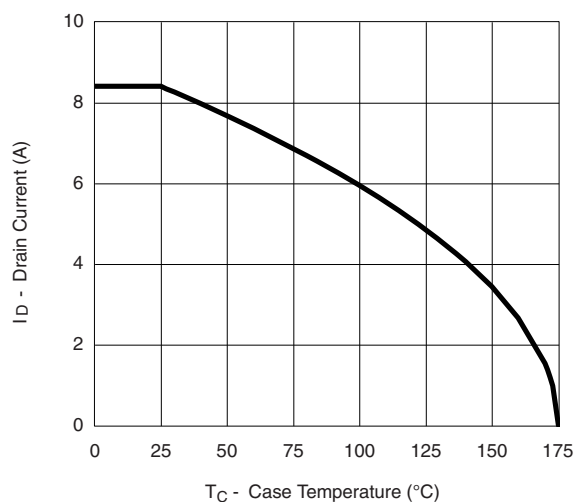
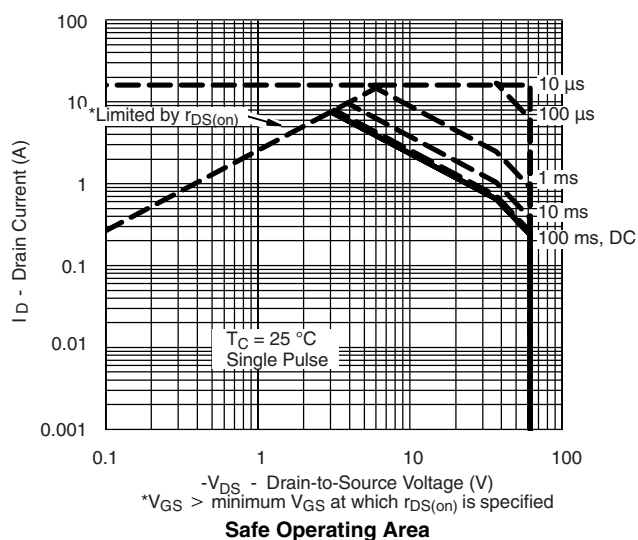
- a. Guaranteed by design, not subject to production testing.  
 b. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
 c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## TYPICAL CHARACTERISTICS 25 °C unless noted

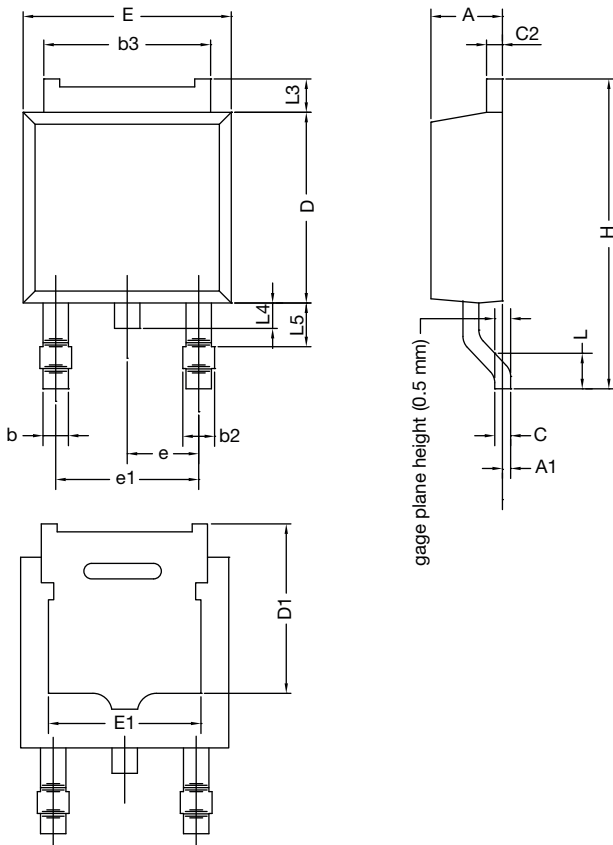


**TYPICAL CHARACTERISTICS** 25 °C unless noted

**On-Resistance vs. Junction Temperature**

**Source-Drain Diode Forward Voltage**
**THERMAL RATINGS**

**Drain Current vs. Case Temperature**

**Safe Operating Area**

**THERMAL RATINGS****Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case**

## TO-252AA CASE OUTLINE



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.14	1.52	0.045	0.060
ECN: X12-0247-Rev. M, 24-Dec-12				
DWG: 5347				

### Note

- Dimension L3 is for reference only.

## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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