

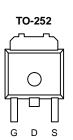
### IRFR13N15DTR-VB Datasheet N-Channel 150 V (D-S) MOSFET

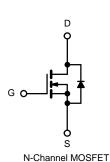
PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)		
150	$0.074 \text{ at V}_{GS} = 10 \text{ V}$	25.4	23 nC		
150	0.077 at V <sub>GS</sub> = 8 V	22.5	23 110		

#### **FEATURES**

- Halogen-free According to IEC 61249-2-21 Definition
- Extremely Low Q<sub>gd</sub> for Switching Losses
- 100 % R<sub>g</sub> Tested
- 100 % Avalanche Tested
- Compliant to RoHS Directive 2002/95/EC







#### **APPLICATIONS**

· Primary Side Switch

Parameter	Symbol	Limit	Unit		
Drain-Source Voltage		V <sub>DS</sub>	150	V	
Gate-Source Voltage		V <sub>GS</sub>	± 20		
	T <sub>C</sub> = 25 °C		25.4		
Continuous Drain Current (T. 150 °C)	T <sub>C</sub> = 70 °C	1 , —	23.1		
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C	l <sub>D</sub>	15.5 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C	1	14.5 <sup>b, c</sup>	Α	
Pulsed Drain Current		I <sub>DM</sub>	50		
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C		4.5		
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	Is	2.6 <sup>b, c</sup>		
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	20		
Single Pulse Avalanche Energy		E <sub>AS</sub>	20	mJ	
	T <sub>C</sub> = 25 °C		5.9		
Maximum Power Discinction	T <sub>C</sub> = 70 °C		3.8	W	
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	3.1 <sup>b, c</sup>	VV	
	T <sub>A</sub> = 70 °C	1	2 <sup>b, c</sup>		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stq</sub>	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS								
Parameter		Symbol	Typical	Maximum	Unit			
Maximum Junction-to-Ambient <sup>b, †</sup>	t ≤ 10 s	R <sub>thJA</sub>	33	40	°C/W			
Maximum Junction-to-Foot (Drain)	Steady State	R <sub>thJF</sub>	17	21	- C/VV			

#### Notes

- a. Based on  $T_C = 25$  °C.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. Maximum under steady state conditions is 80 °C/W.



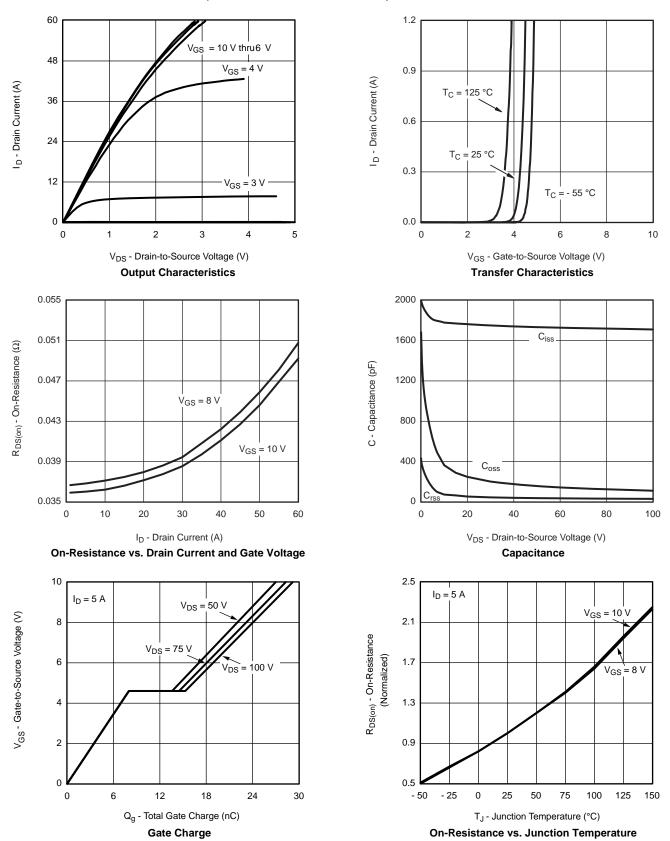
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	150			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	c/T.		172		mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA		- 10		l mv/·C	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_{D} = 250 \mu A$	1.5		3.0	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zara Cata Valtaga Drain Current		V <sub>DS</sub> = 150 V, V <sub>GS</sub> = 0 V			1		
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = 120 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			10	μA	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	30			Α	
Drain Source On State Registered	В	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5 A		0.074			
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 8 V, I <sub>D</sub> = 5 A		0.077		Ω	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 5 A		23		S	
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>			1735			
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		160		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>			37			
Total Gate Charge	Q <sub>g</sub>	$V_{DS} = 75 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 5 \text{ A}$		28.5	43		
Total Gate Charge				23	35	nC	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 75 \text{ V}, V_{GS} = 8 \text{ V}, I_{D} = 5 \text{ A}$		8			
Gate-Drain Charge	$Q_{gd}$			6.5			
Gate Resistance	$R_{g}$	f = 1 MHz	0.89		1.3	Ω	
Turn-on Delay Time	t <sub>d(on)</sub>			14	21		
Rise Time	t <sub>r</sub>	$V_{DD} = 50 \text{ V}, R_L = 10 \Omega$		12	18		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 5 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		22	33		
Fall Time	t <sub>f</sub>			6	10	ne	
Turn-On Delay Time	t <sub>d(on)</sub>			16	24	ns	
Rise Time	t <sub>r</sub>	$V_{DD}$ = 50 V, $R_L$ = 10 $\Omega$		12	18		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 5 \text{ A}, V_{GEN} = 8 \text{ V}, R_g = 1 \Omega$		20	30		
Fall Time	t <sub>f</sub>			7	12		
<b>Drain-Source Body Diode Characteristi</b>	cs						
Continuous Source-Drain Diode Current	I <sub>S</sub>	$T_C = 25  ^{\circ}C$			7.7	Α	
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				50		
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 2.6 A		0.77	1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			63	95	ns	
Body Diode Reverse Recovery Charge				110	165	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	$_{1F} = 3 \text{ A}$ , $_{11}$ $_{100}$ $_{17}$ $_{15}$ $_{15}$ $_{15}$ $_{15}$		49		ns	
Reverse Recovery Rise Time	t <sub>b</sub>			14			

#### Notes:

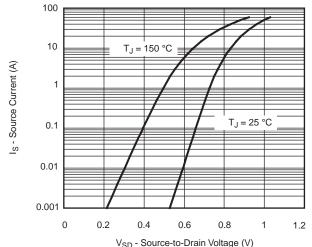
- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%$
- a. Guaranteed by design, not subject to production testing.

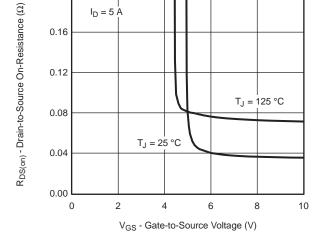
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.





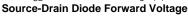


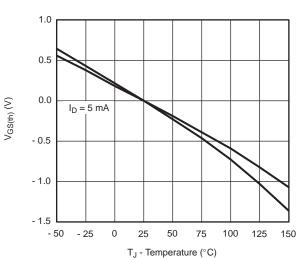




0.20

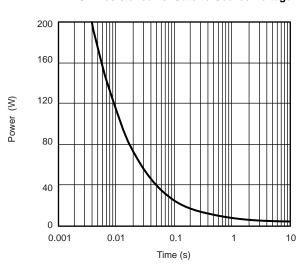
 $I_D = 5 \text{ A}$ 



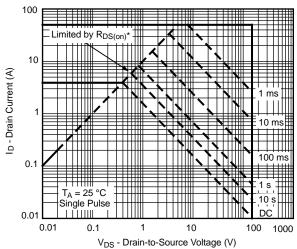


**Threshold Voltage** 

On-Resistance vs. Gate-to-Source Voltage



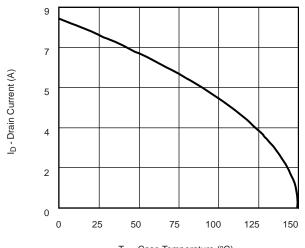
Single Pulse Power, Junction-to-Ambient



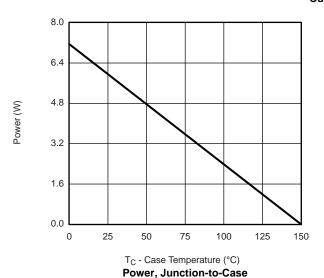
\*  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

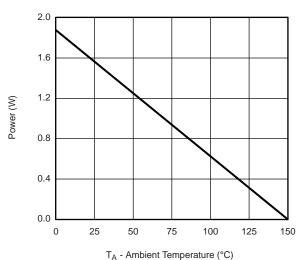
Safe Operating Area, Junction-to-Ambient





T<sub>C</sub> - Case Temperature (°C) **Current Derating\*** 

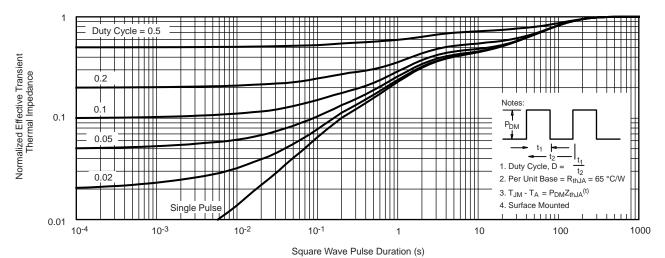




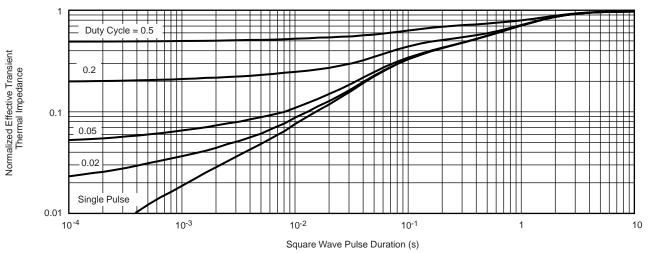
Power, Junction-to-Ambient

<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





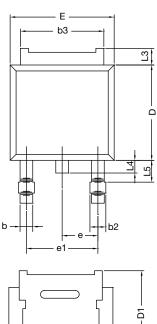
Normalized Thermal Transient Impedance, Junction-to-Ambient

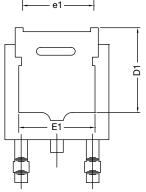


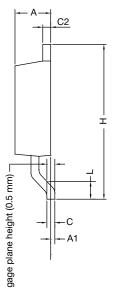
Normalized Thermal Transient Impedance, Junction-to-Foot



## **TO-252AA CASE OUTLINE**







	MILLIMETERS		INC	HES	
DIM.	MIN.	MAX.	MIN.	MAX.	
А	2.18	2.38	0.086	0.094	
A1	-	0.127	-	0.005	
b	0.64	0.88	0.025	0.035	
b2	0.76	1.14	0.030	0.045	
b3	4.95	5.46	0.195	0.215	
С	0.46	0.61	0.018	0.024	
C2	0.46	0.89	0.018	0.035	
D	5.97	6.22	0.235	0.245	
D1	5.21	-	0.205	-	
E	6.35	6.73	0.250	0.265	
E1	4.32	-	0.170	-	
Н	9.40	10.41	0.370	0.410	
е	2.28 BSC		0.090 BSC		
e1	4.56 BSC		0.180 BSC		
L	1.40	1.78	0.055	0.070	
L3	0.89	1.27	0.035	0.050	
L4	-	1.02	-	0.040	
L5	1.14	1.52	0.045	0.060	
ECN: X12-0247-Rev. M, 24-Dec-12					

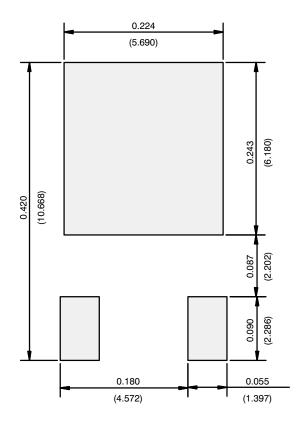
ECN: X12-0247-Rev. M, 24-Dec-12 DWG: 5347

#### Note

• Dimension L3 is for reference only.



### **RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)**



Recommended Minimum Pads Dimensions in Inches/(mm)



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