

## IRFR12N25DCTRLP-VB Datasheet

### N-Channel 250 V (D-S) 175 °C MOSFET

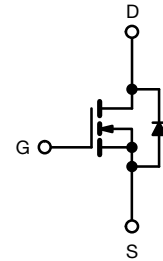
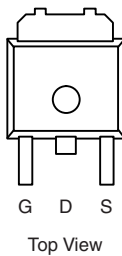
PRODUCT SUMMARY		
$V_{DS}$ (V)	250	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	0.176
$Q_g$ max. (nC)	68	
$Q_{gs}$ (nC)	11	
$Q_{gd}$ (nC)	35	
Configuration	Single	

#### FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- Fast switching
- Ease of paralleling
- Simple drive requirements



TO-252



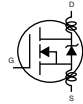

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)						
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V <sub>DS</sub>	250	V	
Gate-Source Voltage			V <sub>GS</sub>	± 20		
Continuous Drain Current	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	I <sub>D</sub>	17	A	
		T <sub>C</sub> = 100 °C		11		
Pulsed Drain Current <sup>a</sup>			I <sub>DM</sub>	56		
Linear Derating Factor				1.0	W/°C	
Single Pulse Avalanche Energy <sup>b</sup>			E <sub>AS</sub>	550	mJ	
Repetitive Avalanche Current <sup>a</sup>			I <sub>AR</sub>	17	A	
Repetitive Avalanche Energy <sup>a</sup>			E <sub>AR</sub>	13	mJ	
Maximum Power Dissipation		T <sub>C</sub> = 25 °C		P <sub>D</sub>	125	W
Peak Diode Recovery dV/dt <sup>c</sup>			dV/dt	4.8	V/ns	
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C	
Soldering Recommendations (Peak temperature) <sup>d</sup>		for 10 s		300		
Mounting Torque	6-32 or M3 screw			10	lbf · in	
				1.1	N · m	

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
 b.  $V_{DS} = 50\text{ V}$ , starting  $T_J = 25\text{ }^{\circ}\text{C}$ ,  $L = 4.5\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 14\text{ A}$  (see fig. 12).  
 c.  $I_{SD} \leq 14\text{ A}$ ,  $dI/dt \leq 150\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^{\circ}\text{C}$ .  
 d. 1.6 mm from case.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.50	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.0	

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		250	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.34	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 250 V, V <sub>GS</sub> = 0 V		-	-	25	μA
		V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	250	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 8.4 A <sup>b</sup>	-	0.176	-	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 8.4 A <sup>b</sup>		6.7	-	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5		-	1300	-	pF
Output Capacitance	C <sub>oss</sub>			-	330	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	85	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 7.9 A, V <sub>DS</sub> = 200 V, see fig. 6 and 13 <sup>b</sup>	-	-	68	nC
Gate-Source Charge	Q <sub>gs</sub>			-	-	11	
Gate-Drain Charge	Q <sub>gd</sub>			-	-	35	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 125 V, I <sub>D</sub> = 7.9 A, R <sub>g</sub> = 9.1 Ω, R <sub>D</sub> = 8.7 Ω, see fig. 10 <sup>b</sup>		-	11	-	ns
Rise Time	t <sub>r</sub>			-	24	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	53	-	
Fall Time	t <sub>f</sub>			-	49	-	
Internal Drain Inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	L <sub>S</sub>			-	7.5	-	
Gate Input Resistance	R <sub>g</sub>	f = 1 MHz, open drain		0.3	-	1.2	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	14	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	56	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 14 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	1.8	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 7.9 A, dI/dt = 100 A/μs <sup>b</sup>		-	250	500	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	2.3	4.6	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

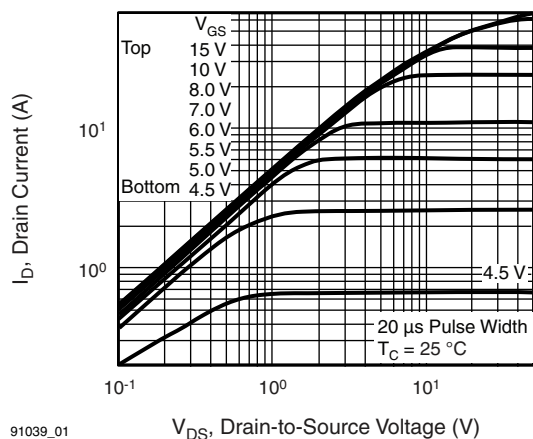


Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^{\circ}\text{C}$

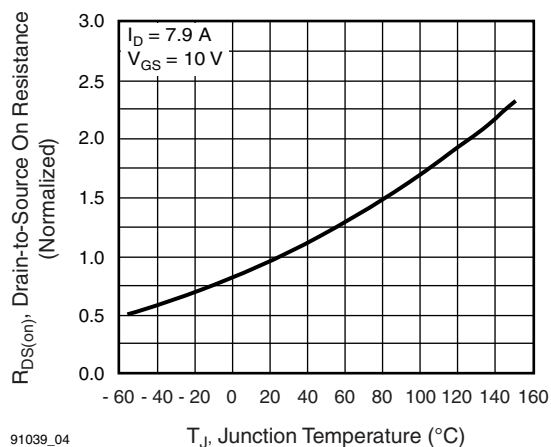


Fig. 4 - Normalized On-Resistance vs. Temperature

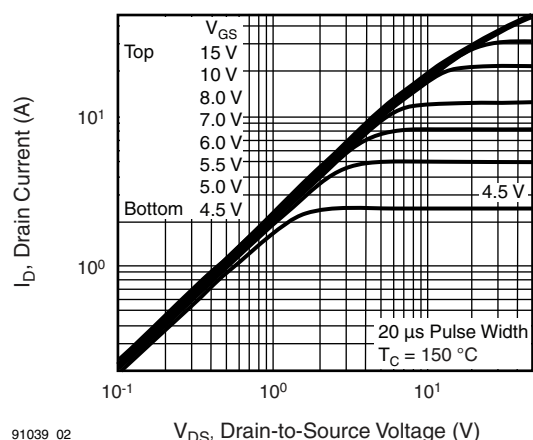


Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^{\circ}\text{C}$

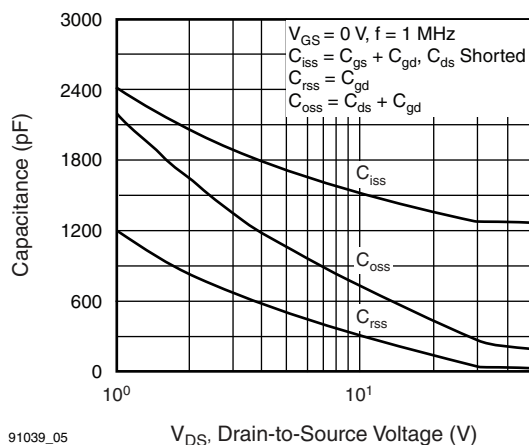


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

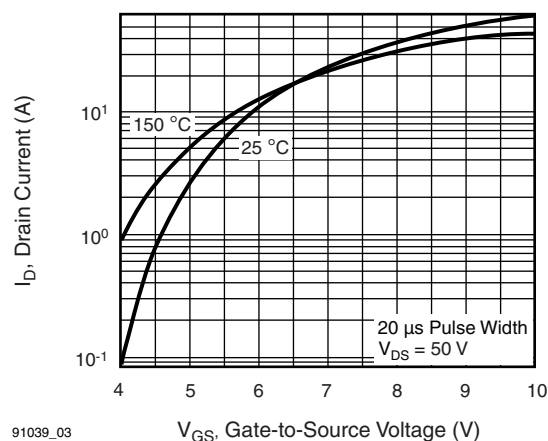


Fig. 3 - Typical Transfer Characteristics

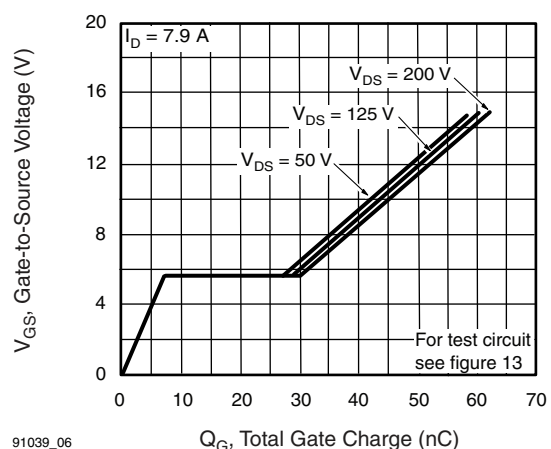
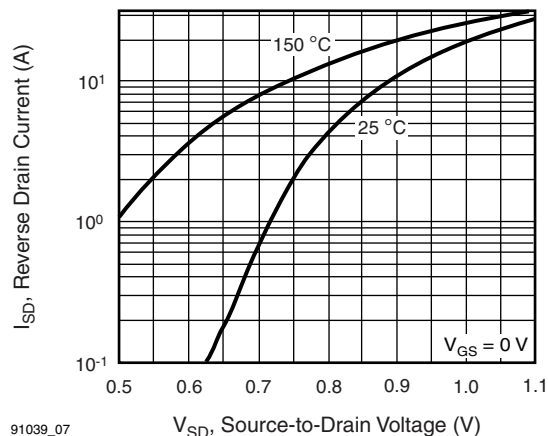
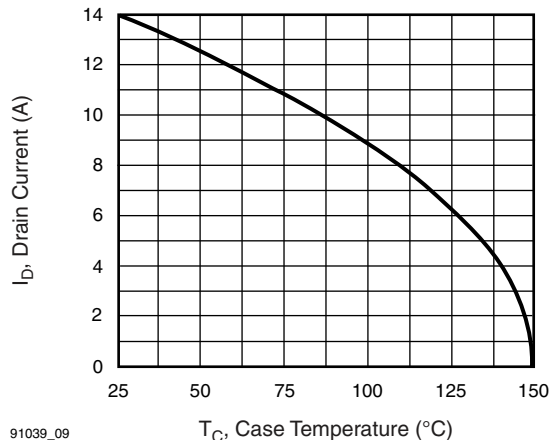


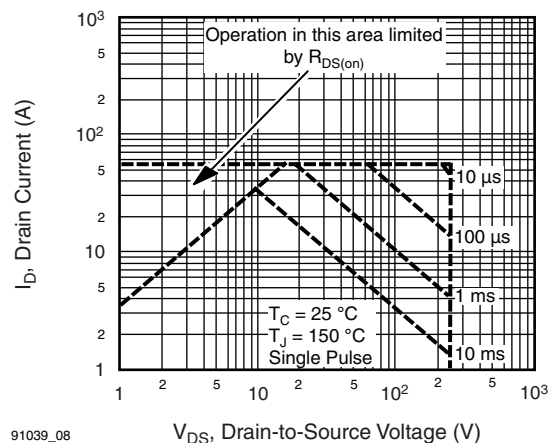
Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



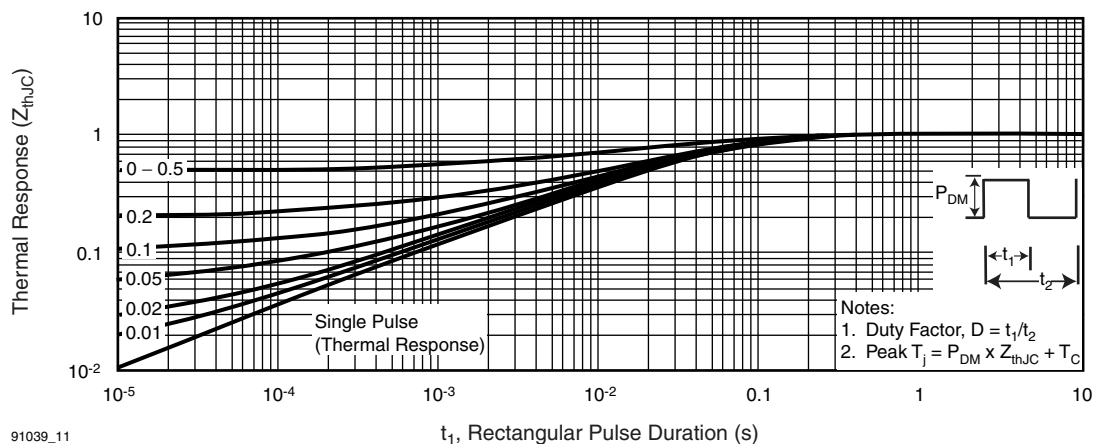
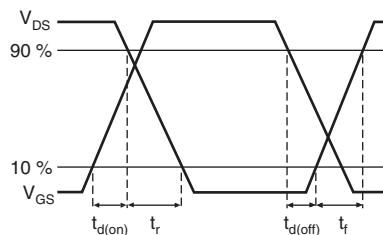
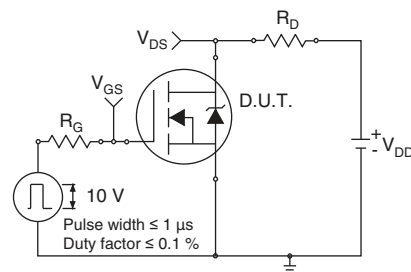
**Fig. 7 - Typical Source-Drain Diode Forward Voltage**



**Fig. 9 - Maximum Drain Current vs. Case Temperature**



**Fig. 8 - Maximum Safe Operating Area**



**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

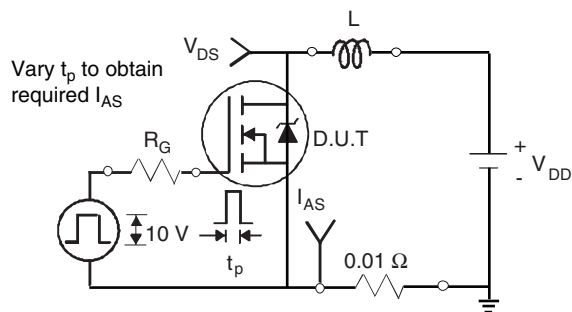


Fig. 12a - Unclamped Inductive Test Circuit

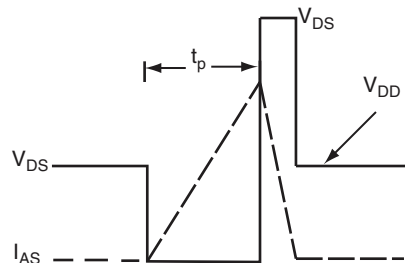


Fig. 12b - Unclamped Inductive Waveforms

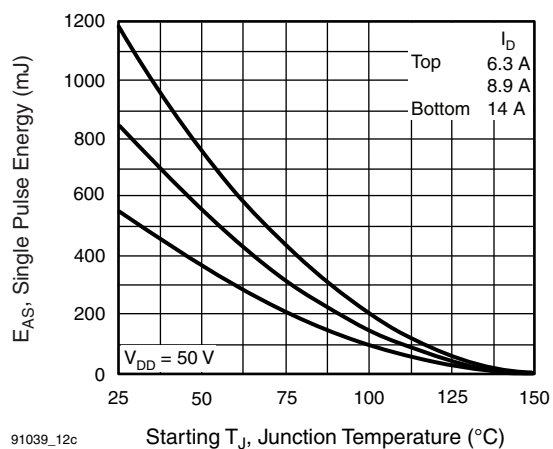


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

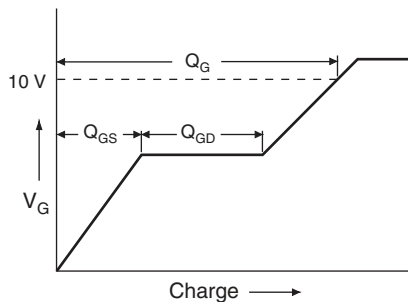


Fig. 13a - Basic Gate Charge Waveform

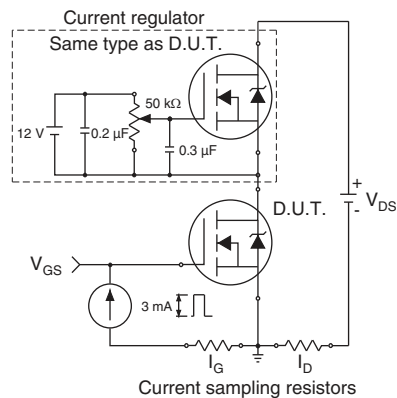
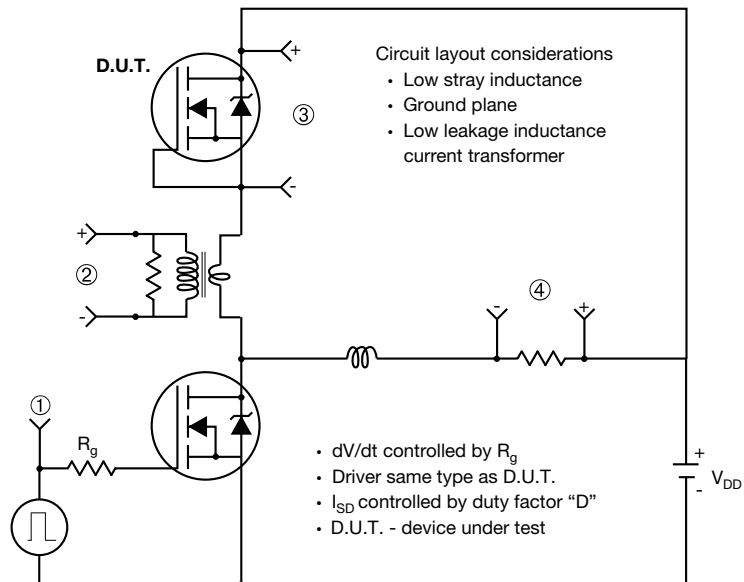


Fig. 13b - Gate Charge Test Circuit

## Peak Diode Recovery dV/dt Test Circuit



### Note

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

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