

# IPD80N04S3-06-VB Datasheet N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	$R_{DS(on)}$ ( $\Omega$ )	I <sub>D</sub> (A) <sup>a, c</sup>	Q <sub>g</sub> (Typ.)	
40	0.0050 at V <sub>GS</sub> = 10 V	85	80 nC	
	0.0065 at V <sub>GS</sub> = 4.5 V	70	00110	

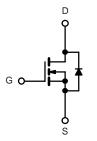
#### **FEATURES**

- Trench Power MOSFET
- 100 %  $R_g$  and UIS Tested



#### **APPLICATIONS**

- Synchronous Rectification
- Power Supplies



N-Channel MOSFET

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<b>ABSOLUTE MAXIMUM RATING</b>	<b>S</b> T <sub>A</sub> = 25 °C, unle	ss otherwise n	oted		
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V <sub>DS</sub>	40	V		
Gate-Source Voltage		V <sub>GS</sub>	± 25	V	
	T <sub>C</sub> = 25 °C		85 <sup>a, c</sup>		
Continuous Drain Current (T <sub>.I</sub> = 175 °C)	T <sub>C</sub> = 70 °C		70 <sup>c</sup>		
Continuous Diain Current (1) = 173 C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	59 <sup>b</sup>	Α	
	T <sub>A</sub> = 70 °C		53 <sup>b</sup>	A	
Pulsed Drain Current	I <sub>DM</sub>	250			
Avalanche Current Pulse L = 0.1 mH		I <sub>AS</sub>			80
Single Pulse Avalanche Energy	L = 0.1 IIII	E <sub>AS</sub>	320	mJ	
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C	L	110 <sup>a, c</sup>	Λ	
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	2.6 <sup>b</sup>	Α	
	T <sub>C</sub> = 25 °C		312 <sup>a</sup>		
Maniana Barras Biasinatian	T <sub>C</sub> = 70 °C	]	200	14/	
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	$P_{D}$	3.13 <sup>b</sup>	W	
	T <sub>A</sub> = 70 °C		2.0 <sup>b</sup>		
Operating Junction and Storage Temperature R	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient <sup>b</sup>	Steady State	R <sub>thJA</sub>	32	40	°C/W	
Maximum Junction-to-Case	Steady State	$R_{thJC}$	0.33	0.4	]	

#### Notes:

- a. Based on  $T_C = 25$  °C.
- b. Surface Mounted on 1" x 1" FR4 board.
- c. Calculated based on maximum junction temperature. Package limitation current is 110  $\,\mathrm{A.}$



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	40			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	L = 250 µA		41		m\//ºC	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_{J}$	In = 750 HA		- 8		mV/°C	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.2		2.5	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zoro Coto Voltago Proin Current	l	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$			1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			10	μA	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	120			Α	
David Course Co. Otata Basista and	D	$V_{GS} = 10 \text{ V}, I_D = 30 \text{ A}$		0.0050			
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$		0.0065		Ω	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	$V_{DS} = 15 \text{ V}, I_{D} = 30 \text{ A}$		180		S	
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>			2380		pF	
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		550			
Reverse Transfer Capacitance	C <sub>rss</sub>			250			
Total Gate Charge	$Q_g$			80	120	nC	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 20 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 20 \text{ A}$		20			
Gate-Drain Charge	$Q_{gd}$			12			
Gate Resistance	R <sub>g</sub>	f = 1 MHz		0.85	1.3	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			20	30		
Rise Time	t <sub>r</sub>	$V_{DD}$ = 20 V, $R_L$ = 1.0 $\Omega$		11	17	1	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D\cong 20$ A, $V_{GEN}$ = 10 V, $R_g$ = 1 $\Omega$		77	115		
Fall Time	t <sub>f</sub>			10	15		
Turn-On Delay Time	t <sub>d(on)</sub>			102	155	ns	
Rise Time	t <sub>r</sub>	$V_{DD}$ = 20 V, $R_L$ = 1.0 $\Omega$		62	95		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D\cong 20$ A, $V_{GEN}$ = 4.5 V, $R_g$ = 1 $\Omega$		180	270		
Fall Time	t <sub>f</sub>			60	90		
<b>Drain-Source Body Diode Characteristic</b>	s					I	
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			110	^	
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				200	A	
Body Diode Voltage	$V_{SD}$	I <sub>S</sub> = 20 A		0.8	1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			50	75	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	L = 20 A di/dt = 100 A/vo T = 25 °C		70	105	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	I <sub>F</sub> = 20 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C		30			
Reverse Recovery Rise Time	t <sub>b</sub>			20		ns	

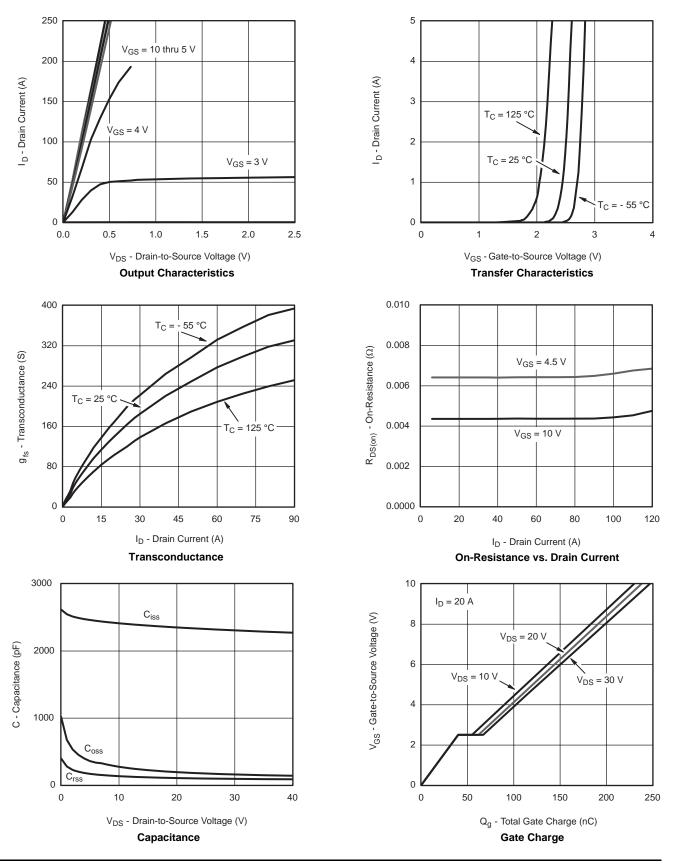
#### Notes:

- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

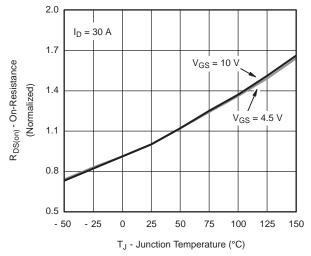


#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

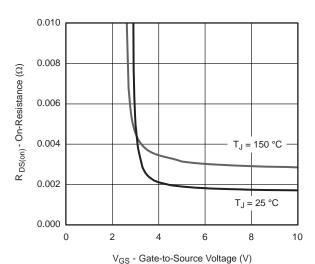




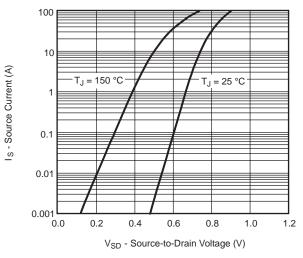
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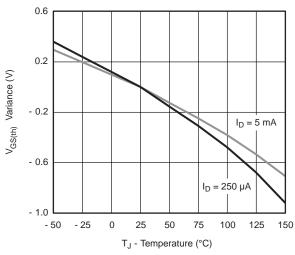
#### On-Resistance vs. Junction Temperature



On-Resistance vs. Gate-to-Source Voltage



#### Forward Diode Voltage vs. Temperature



#### Threshold Voltage

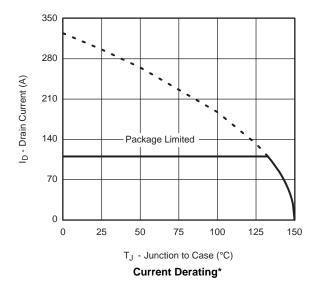


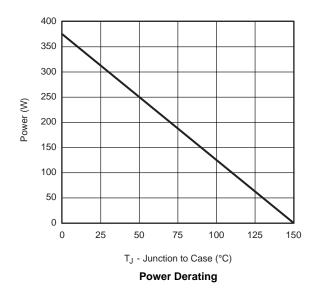
 $^{\star}$  V  $_{GS}$  > minimum V  $_{GS}$  at which R  $_{DS(on)}$  is specified

Safe Operating Area, Junction-to-Ambient

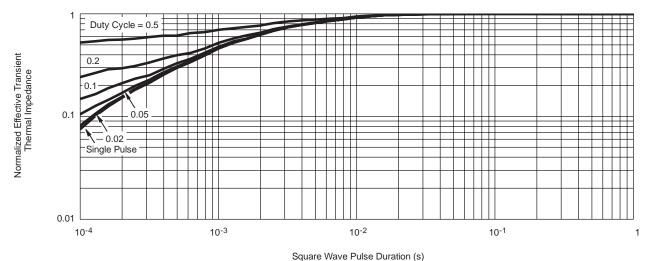


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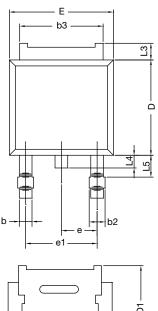
<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max)}$  = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

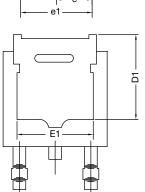


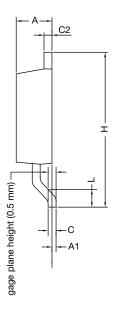
Normalized Thermal Transient Impedance, Junction-to-Case



## **TO-252AA CASE OUTLINE**







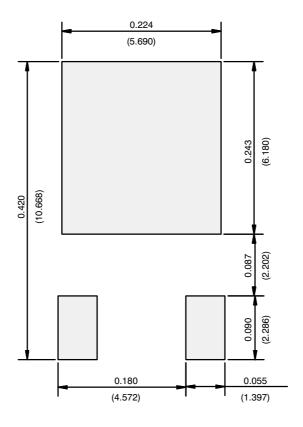
	MILLIMETERS		INC	HES
DIM.	MIN.	MAX.	MIN.	MAX.
Α	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
С	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.21	-	0.205	=
Е	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	=
Н	9.40	10.41	0.370	0.410
е	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.14	1.52	0.045	0.060
ECN: X12-0247-Rev. M, 24-Dec-12 DWG: 5347				

#### Note

• Dimension L3 is for reference only.



#### **RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)**



Recommended Minimum Pads Dimensions in Inches/(mm)



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