# HFD1N80-VB Datasheet

## N-Channel 800V (D-S) Super Junction Power MOSFET

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) at $T_J$ max. | 800 | |
| $R_{DS(on)}$ typ. (Ω) at 25 °C | $V_{GS}$ = 10 V | 2.38 |
| $Q_g$ max. (nC) | 90 | |
| $Q_{gs}$ (nC) | 11 | |
| $Q_{gd}$ (nC) | 19 | |
| Configuration | Single | |

### FEATURES

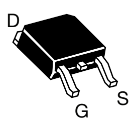
- Low figure-of-merit (FOM) $R_{on}$ x $Q_g$
- Low input capacitance ($C_{iss}$)
- Reduced switching and conduction losses
- Ultra low gate charge ($Q_g$)
- Avalanche energy rated (UIS)

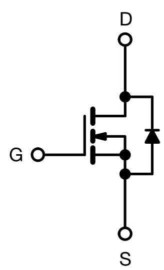
RoHS COMPLIANT
HALOGEN FREE

### APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Renewable energy
  - Solar (PV inverters)

**DPAK (TO-252)**



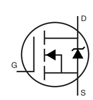

N-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS ($T_C$ = 25 °C, unless otherwise noted) | | | | | |
|---|---|---|---|---|---|
| **PARAMETER** | | | **SYMBOL** | **LIMIT** | **UNIT** |
| Drain-source voltage | | | $V_{DS}$ | 800 | V |
| Gate-source voltage | | | $V_{GS}$ | ± 30 | |
| Continuous drain current ($T_J$ = 150 °C) | $V_{GS}$ at 10 V | $T_C$ = 25 °C | $I_D$ | 2.8 | A |
| | | $T_C$ = 100 °C | | 1.8 | |
| Pulsed drain current [a] | | | $I_{DM}$ | 5 | |
| Linear derating factor | | | | 0.5 | W/°C |
| Single pulse avalanche energy [b] | | | $E_{AS}$ | 14 | mJ |
| Maximum power dissipation | | | $P_D$ | 62.5 | W |
| Operating junction and storage temperature range | | | $T_J$, $T_{stg}$ | -55 to +150 | °C |
| Drain-source voltage slope | $T_J$ = 125 °C | | dV/dt | 70 | V/ns |
| Reverse diode dV/dt [d] | | | | 0.13 | |
| Soldering recommendations (peak temperature) [c] | For 10 s | | | 300 | °C |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature
b. $V_{DD}$ = 140 V, starting $T_J$ = 25 °C, L = 28.2 mH, $R_g$ = 25 Ω, $I_{AS}$ = 0.9 A
c. 1.6 mm from case
d. $I_{SD} \leq I_D$, dI/dt = 100 A/μs, starting $T_J$ = 25 °C

| THERMAL RESISTANCE RATINGS | | | | |
|---|---|---|---|---|
| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
| Maximum junction-to-ambient | $R_{thJA}$ | - | 62 | °C/W |
| Maximum junction-to-case (drain) | $R_{thJC}$ | - | 2.0 | |

| SPECIFICATIONS ($T_J$ = 25 °C, unless otherwise noted) | | | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| **Static** | | | | | | |
| Drain-source breakdown voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 μA | 800 | - | - | V |
| $V_{DS}$ temperature coefficient | $\Delta V_{DS}/T_J$ | Reference to 25 °C, $I_D$ = 1 mA | - | 1.0 | - | V/°C |
| Gate-source threshold Voltage (N) | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 2.0 | - | 4.0 | V |
| Gate-source leakage | $I_{GSS}$ | $V_{GS}$ = ± 20 V | - | - | ± 100 | nA |
| | | $V_{GS}$ = ± 30 V | - | - | ± 1 | μA |
| Zero gate voltage drain current | $I_{DSS}$ | $V_{DS}$ = 800 V, $V_{GS}$ = 0 V | - | - | 1 | μA |
| | | $V_{DS}$ = 640 V, $V_{GS}$ = 0 V, $T_J$ = 125 °C | - | - | 10 | |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 1.0 A | - | 2.38 | - | Ω |
| Forward transconductance | $g_{fs}$ | $V_{DS}$ = 30 V, $I_D$ = 1.0 A | - | 1.0 | - | S |
| **Dynamic** | | | | | | |
| Input capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 100 V, f = 1 MHz | - | 315 | - | pF |
| Output capacitance | $C_{oss}$ | | - | 20 | - | |
| Reverse transfer capacitance | $C_{rss}$ | | - | 6 | - | |
| Effective output capacitance, energy related [a] | $C_{o(er)}$ | $V_{DS}$ = 0 V to 480 V, $V_{GS}$ = 0 V | - | 13 | - | |
| Effective output capacitance, time related [b] | $C_{o(tr)}$ | | - | 45 | - | |
| Total gate charge | $Q_g$ | $V_{GS}$ = 10 V, $I_D$ = 1.0 A, $V_{DS}$ = 480 V | - | 9.8 | 19.6 | nC |
| Gate-source charge | $Q_{gs}$ | | - | 2.4 | - | |
| Gate-drain charge | $Q_{gd}$ | | - | 3.9 | - | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}$ = 480 V, $I_D$ = 1.0 A, $V_{GS}$ = 10 V, $R_g$ = 9.1 Ω | - | 11 | 22 | ns |
| Rise time | $t_r$ | | - | 7 | 14 | |
| Turn-off delay time | $t_{d(off)}$ | | - | 19 | 38 | |
| Fall time | $t_f$ | | - | 27 | 54 | |
| Gate input resistance | $R_g$ | f = 1 MHz, open drain | 1.8 | 3.6 | 7.2 | Ω |
| **Drain-Source Body Diode Characteristics** | | | | | | |
| Continuous source-drain diode current | $I_S$ | MOSFET symbol showing the integral reverse p - n junction diode   | - | - | 2.8 | A |
| Pulsed diode forward current | $I_{SM}$ | | - | - | 5 | |
| Diode forward voltage | $V_{SD}$ | $T_J$ = 25 °C, $I_S$ = 11 A, $V_{GS}$ = 0 V | - | - | 1.2 | V |
| Reverse recovery time | $t_{rr}$ | $T_J$ = 25 °C, $I_F$ = $I_S$ = 1.0 A, dI/dt = 100 A/μs, $V_R$ = 25 V | - | 278 | 556 | ns |
| Reverse recovery charge | $Q_{rr}$ | | - | 0.9 | 1.8 | μC |
| Reverse recovery current | $I_{RRM}$ | | - | 5 | - | A |

**Notes**

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as $C_{oss}$ while $V_{DS}$ is rising from 0 % to 80 % $V_{DSS}$

b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 % to 80 % $V_{DSS}$

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

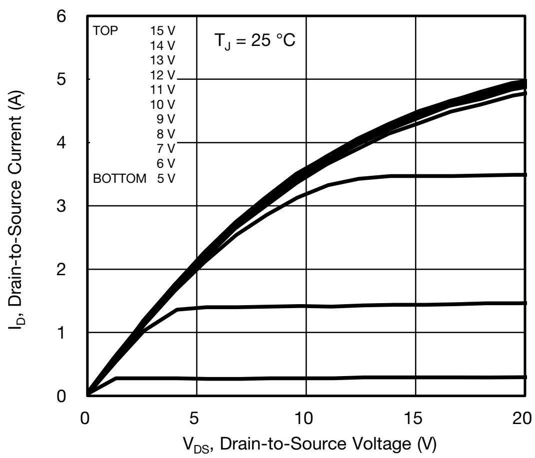



**Fig. 1 - Typical Output Characteristics**

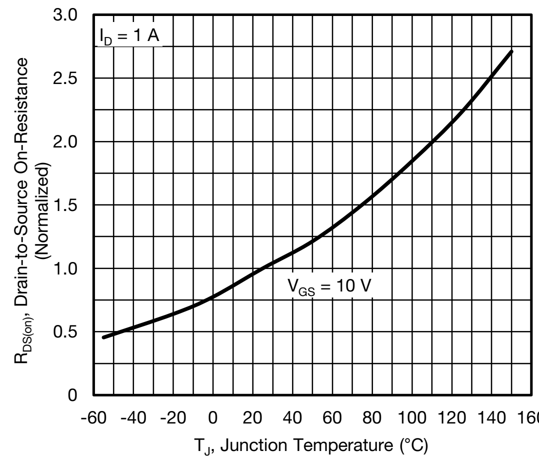



**Fig. 4 - Normalized On-Resistance vs. Temperature**

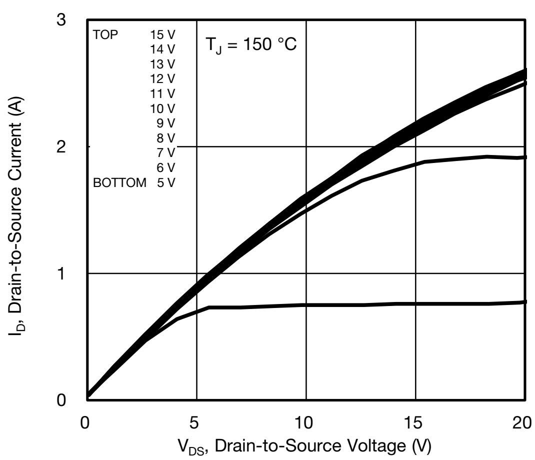



**Fig. 2 - Typical Output Characteristics**

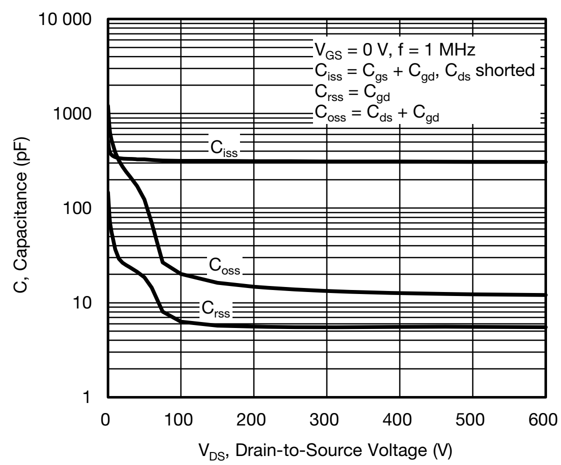



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

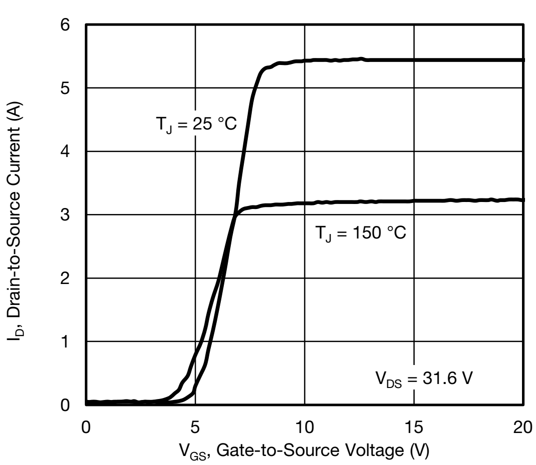



**Fig. 3 - Typical Transfer Characteristics**

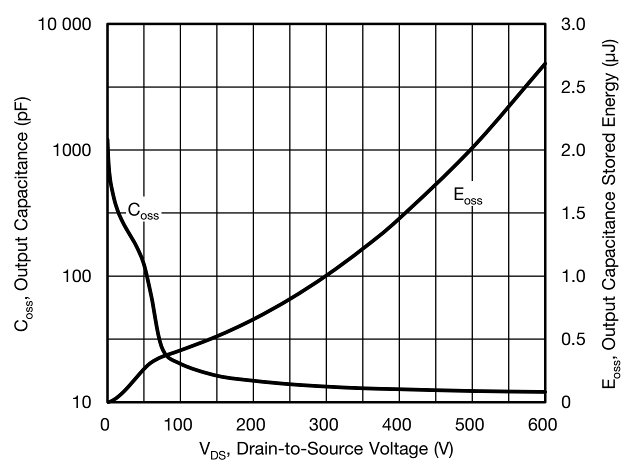



**Fig. 6 - $C_{oss}$ and $E_{oss}$ vs. $V_{DS}$**

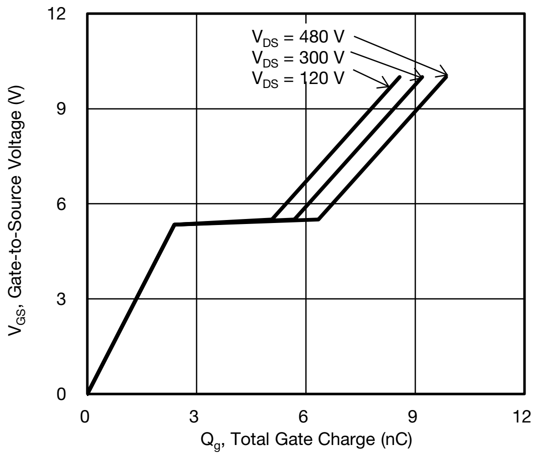



**Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage**

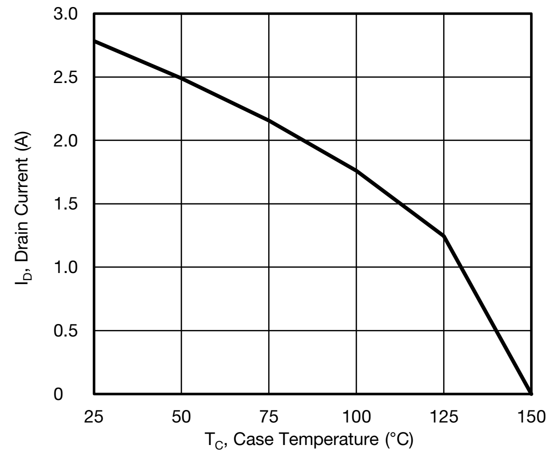



**Fig. 10 - Maximum Drain Current vs. Case Temperature**

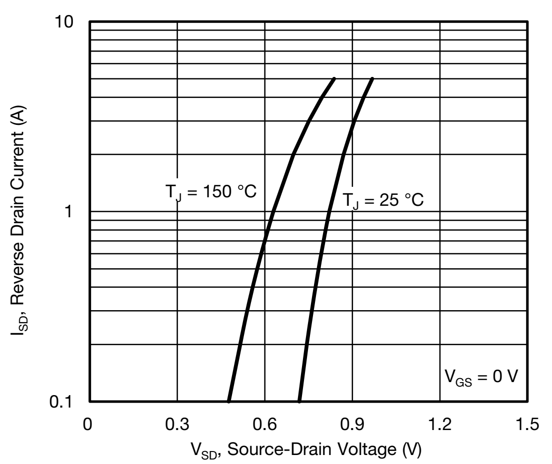



**Fig. 8 - Typical Source-Drain Diode Forward Voltage**

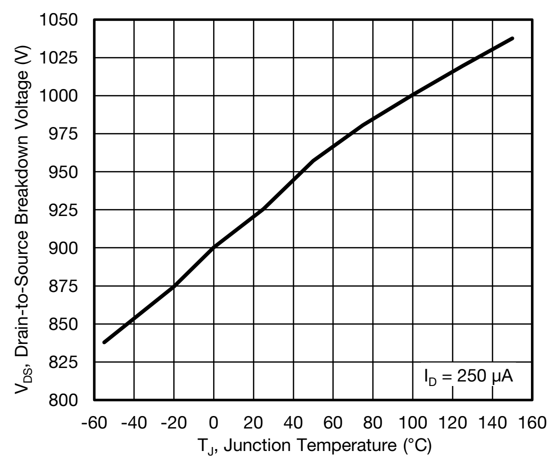
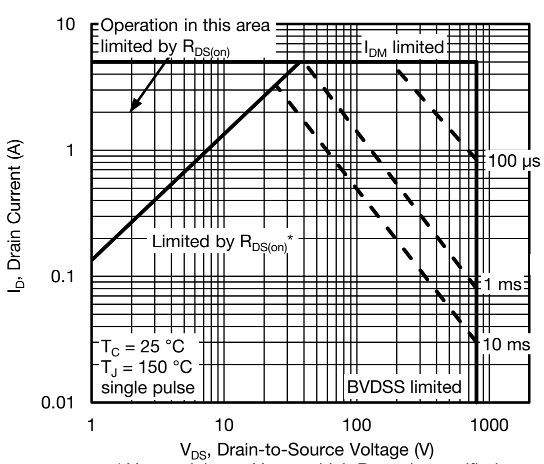



**Fig. 11 - Temperature vs. Drain-to-Source Voltage**




* $V_{GS}$ > minimum $V_{GS}$ at which $R_{DS(on)}$ is specified

**Fig. 9 - Maximum Safe Operating Area**

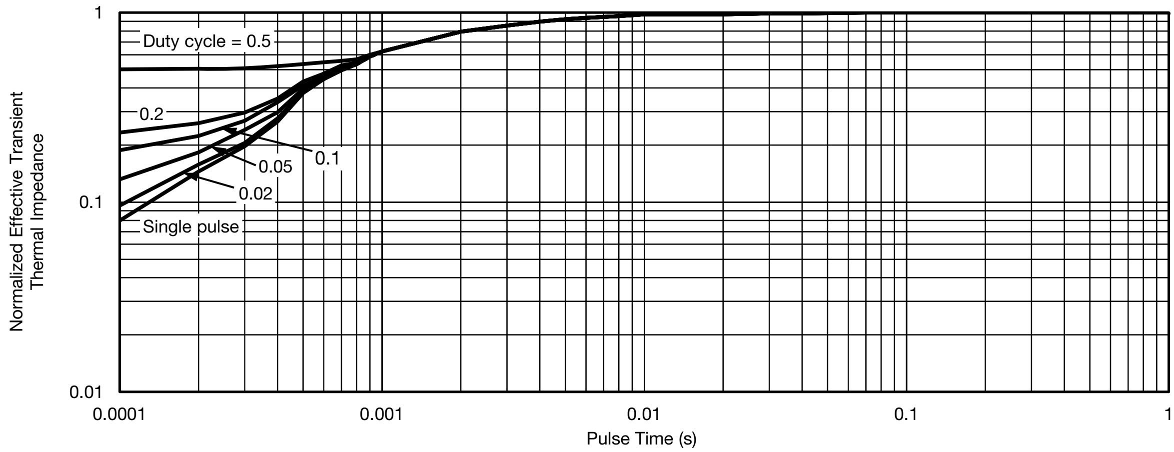



**Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case**

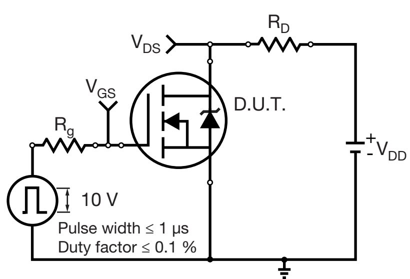



**Fig. 13 - Switching Time Test Circuit**

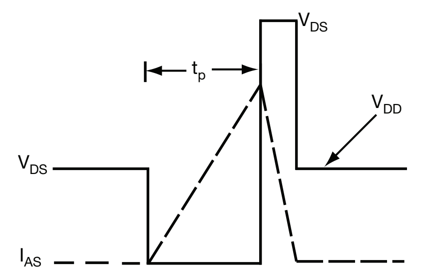



**Fig. 16 - Unclamped Inductive Waveforms**

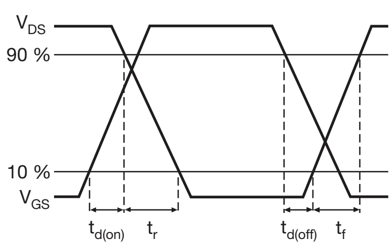



**Fig. 14 - Switching Time Waveforms**

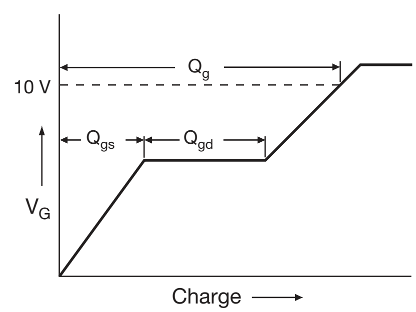



**Fig. 17 - Basic Gate Charge Waveform**

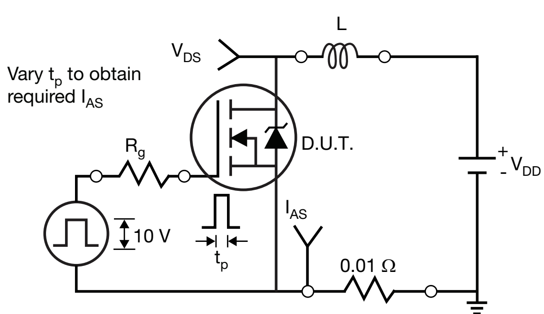



**Fig. 15 - Unclamped Inductive Test Circuit**

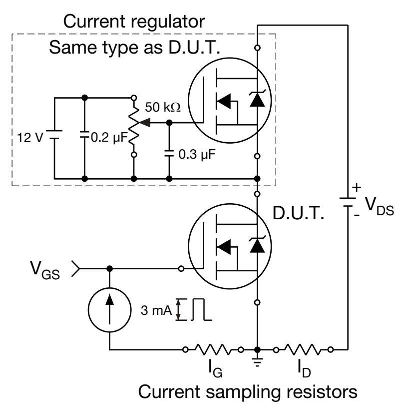
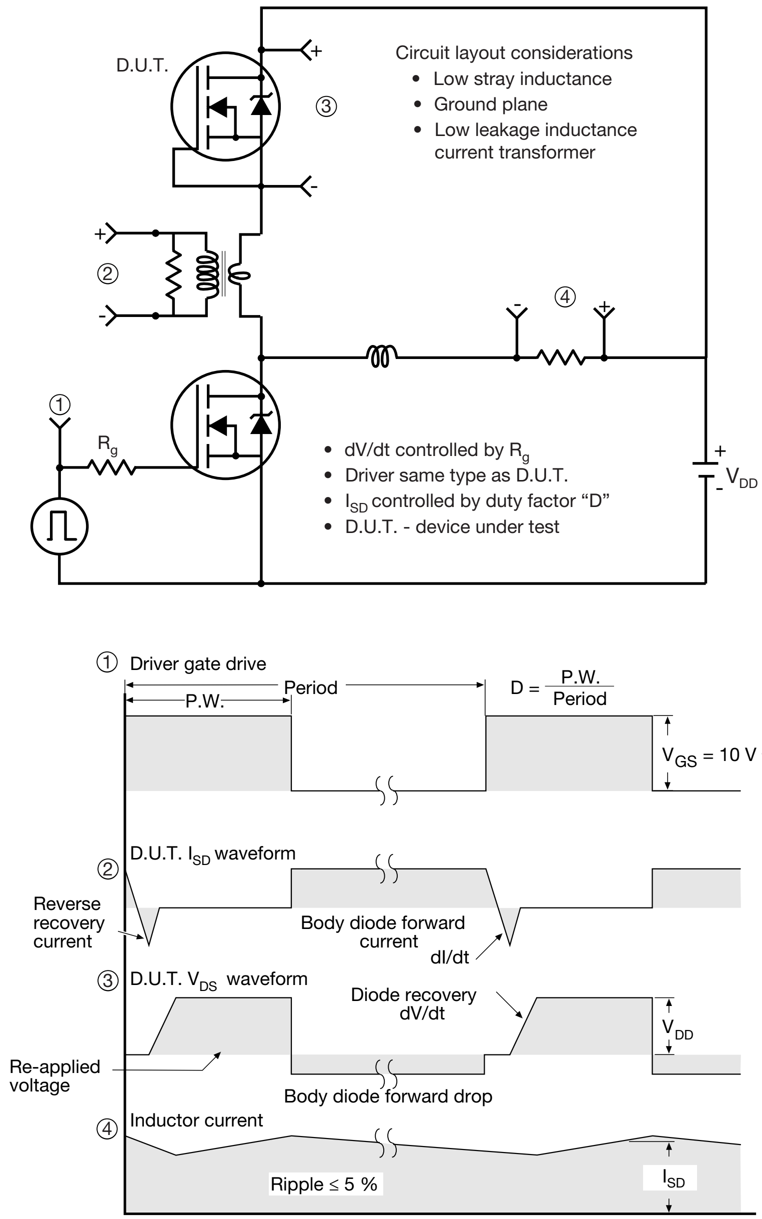



**Fig. 18 - Gate Charge Test Circuit**

**Peak Diode Recovery dV/dt Test Circuit**




**Note**

a. $V_{GS}$ = 5 V for logic level devices

**Fig. 19 - For N-Channel**

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