

## FQD2P25TF-VB Datasheet

### Power MOSFET

#### PRODUCT SUMMARY

$V_{DS}$ (V)	- 250	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = -10\text{ V}$	1.0
$Q_g$ (Max.) (nC)	38	
$Q_{gs}$ (nC)	8.0	
$Q_{gd}$ (nC)	18	
Configuration	Single	

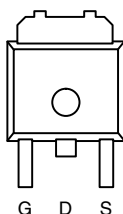
#### FEATURES

- Advanced Process Technology
- Dynamic  $dV/dt$  Rating
- 150 °C Operating Temperature
- Fast Switching
- P-Channel
- Fully Avalanche Rated
- Lead (Pb)-free Available



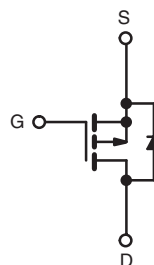
Available  
**RoHS\***  
 COMPLIANT

TO-252



Top View

Drain Connected to Tab



P-Channel MOSFET

#### ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	- 250	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current	$V_{GS}$ at - 10 V	$T_C = 25\text{ }^{\circ}\text{C}$	A
		$T_C = 100\text{ }^{\circ}\text{C}$	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	- 16	
Linear Derating Factor		0.28	W/ $^{\circ}\text{C}$
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	520	mJ
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	- 4.1	A
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	3.5	mJ
Maximum Power Dissipation	$P_D$	85	W
Peak Diode Recovery $dV/dt$ <sup>c</sup>	$dV/dt$	- 5.0	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	$^{\circ}\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

#### Notes


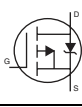
- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting  $T_J = 25\text{ }^{\circ}\text{C}$ ,  $L = 62\text{ mH}$ ,  $R_G = 25\text{ }\Omega$ ,  $I_{AS} = -4.1\text{ A}$  (see fig. 12).
- $I_{SD} \leq -4.1\text{ A}$ ,  $dI/dt \leq -640\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^{\circ}\text{C}$ .
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	65	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	3.6	

**SPECIFICATIONS**  $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		- 250	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	- 0.27	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		- 2.0	-	- 4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = - 250 V, V <sub>GS</sub> = 0 V		-	-	- 25	μA
		V <sub>DS</sub> = - 200 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 150 °C		-	-	- 250	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 10 V	I <sub>D</sub> = - 2.5 A <sup>b</sup>	-	1.0	-	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = - 50 V, I <sub>D</sub> = - 4.1 A <sup>b</sup>		2.2	-	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = - 25 V, f = 1.0 MHz, see fig. 5		-	680	-	pF
Output Capacitance	C <sub>oss</sub>			-	170	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	40	-	
Drain to Sink Capacitance	C	f = 1.0 MHz		-	12	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = - 10 V	I <sub>D</sub> = - 4.1 A, V <sub>DS</sub> = - 200 V, see fig. 6 and 13 <sup>b</sup>	-	-	38	nC
Gate-Source Charge	Q <sub>gs</sub>			-	-	8.0	
Gate-Drain Charge	Q <sub>gd</sub>			-	-	18	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = - 130 V, I <sub>D</sub> = - 4.1 A, R <sub>G</sub> = 12 Ω, R <sub>D</sub> = 31 Ω, see fig. 10 <sup>b</sup>		-	12	-	ns
Rise Time	t <sub>r</sub>			-	23	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	34	-	
Fall Time	t <sub>f</sub>			-	21	-	
Internal Drain Inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	L <sub>S</sub>			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	- 4.1	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	- 16	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = - 4.1 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	- 6.5	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = - 4.1 A, dI/dt = -100 A/μs <sup>b</sup>		-	190	290	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	1.5	2.2	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
 b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

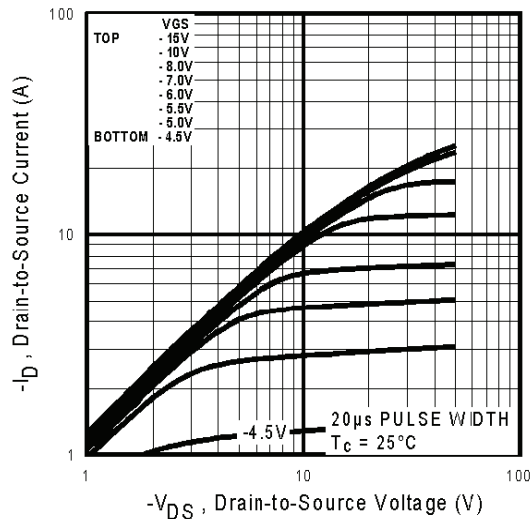


Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^{\circ}\text{C}$

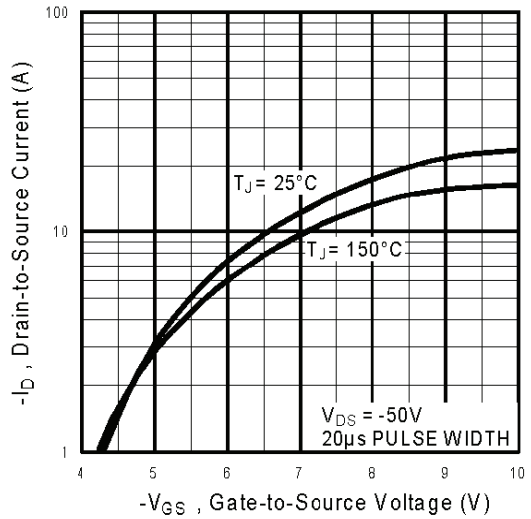


Fig. 3 - Typical Transfer Characteristics

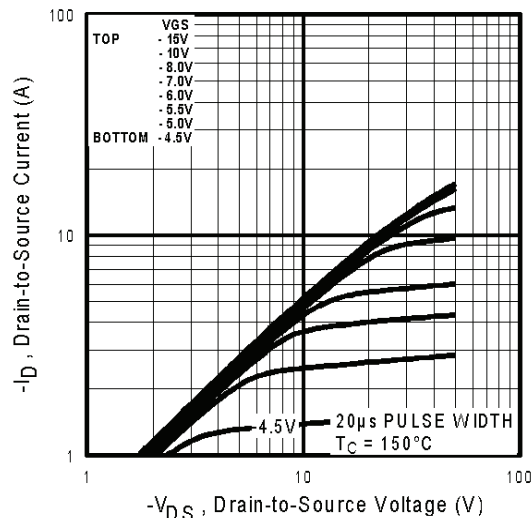


Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^{\circ}\text{C}$

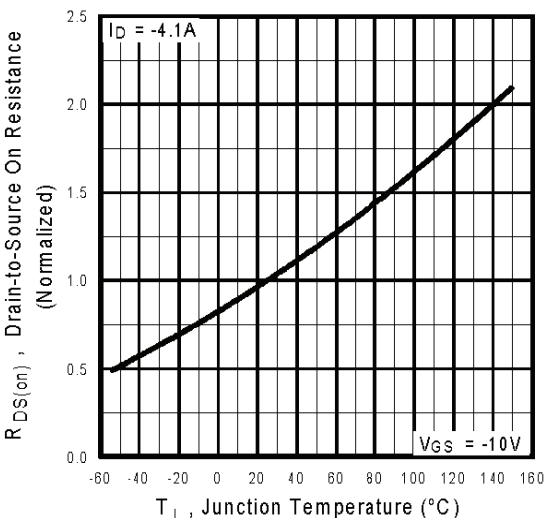


Fig. 4 - Normalized On-Resistance vs. Temperature

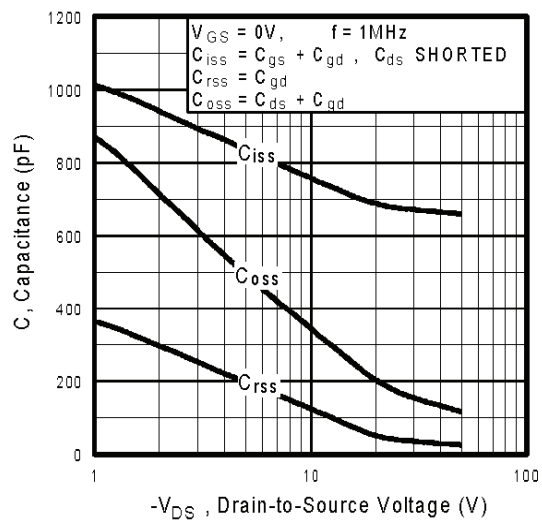


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

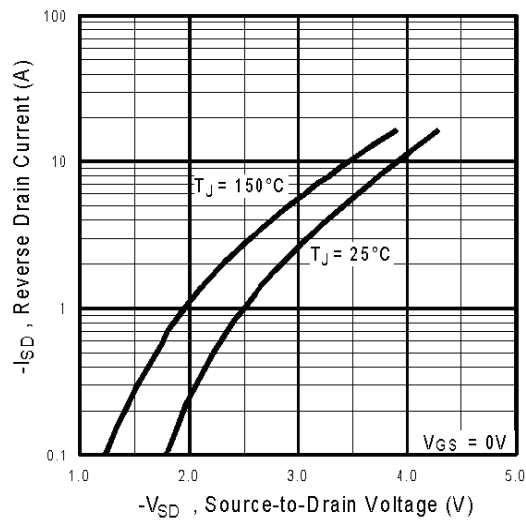


Fig. 7 - Typical Source-Drain Diode Forward Voltage

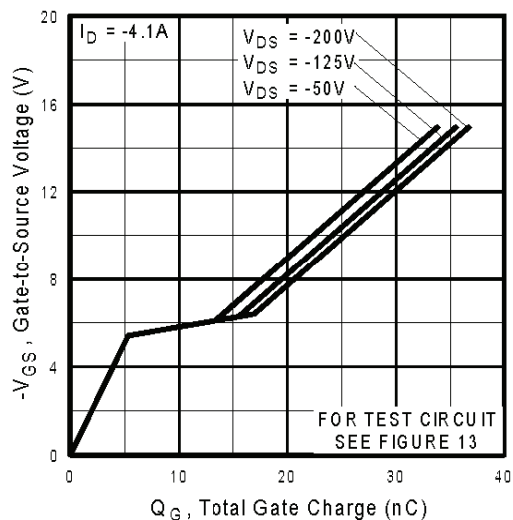


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

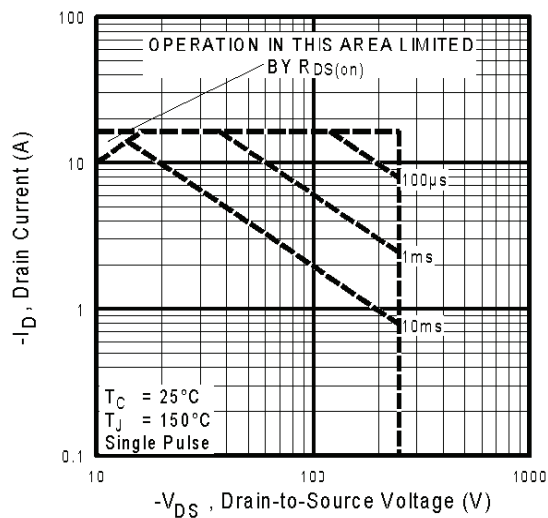


Fig. 8 - Maximum Safe Operating Area



Fig. 9 - Maximum Drain Current vs. Case Temperature

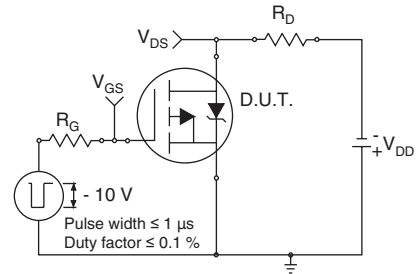


Fig. 10a - Switching Time Test Circuit

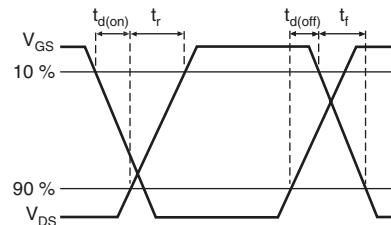


Fig. 10b - Switching Time Waveforms



Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

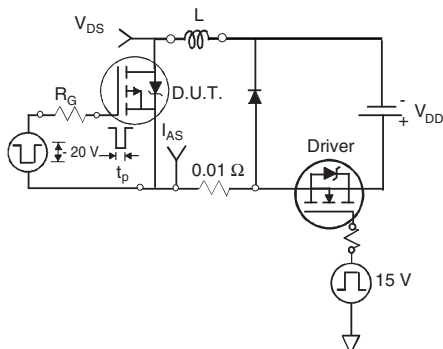


Fig. 12a - Unclamped Inductive Test Circuit

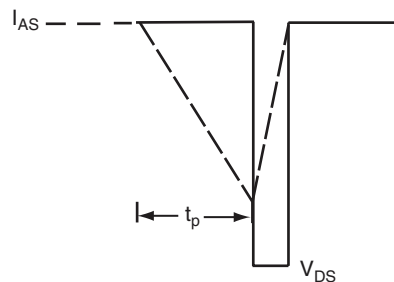


Fig. 12b - Unclamped Inductive Waveforms

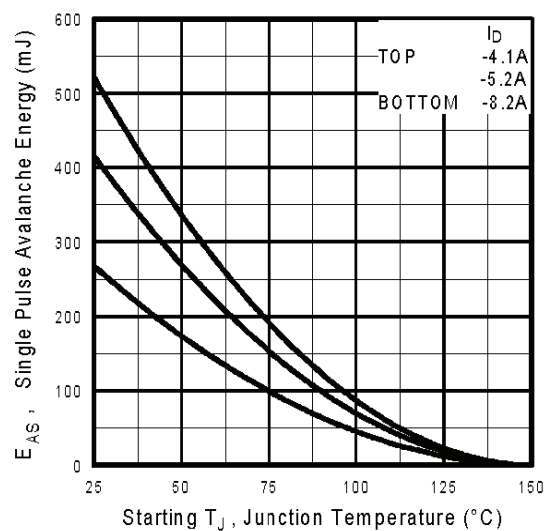


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

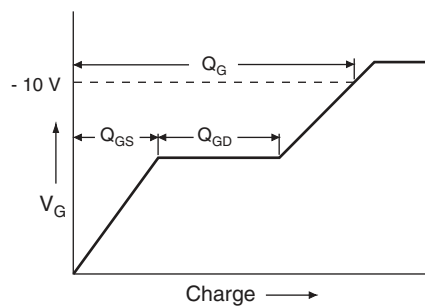


Fig. 13a - Basic Gate Charge Waveform

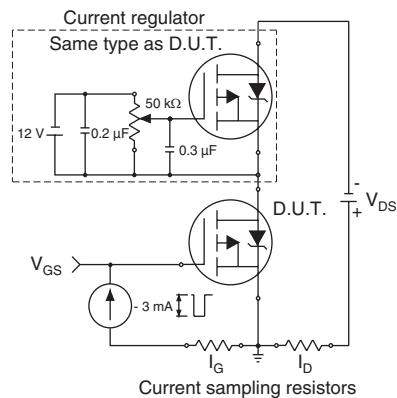
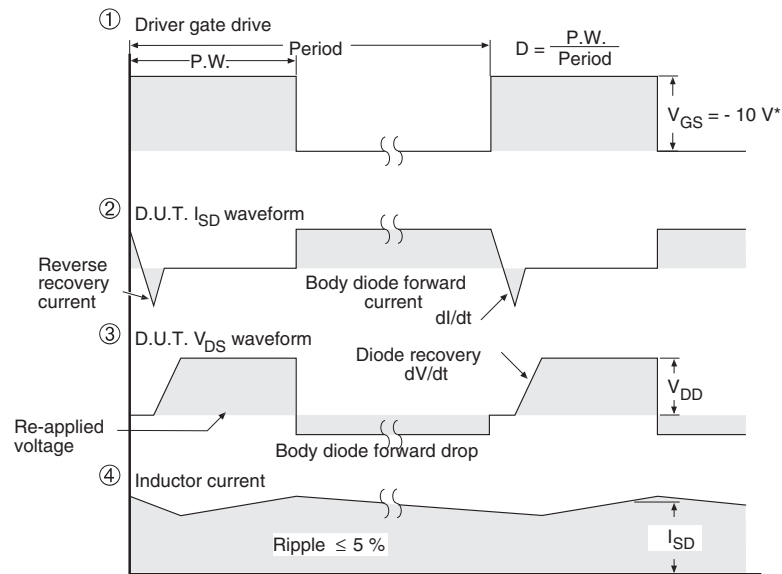
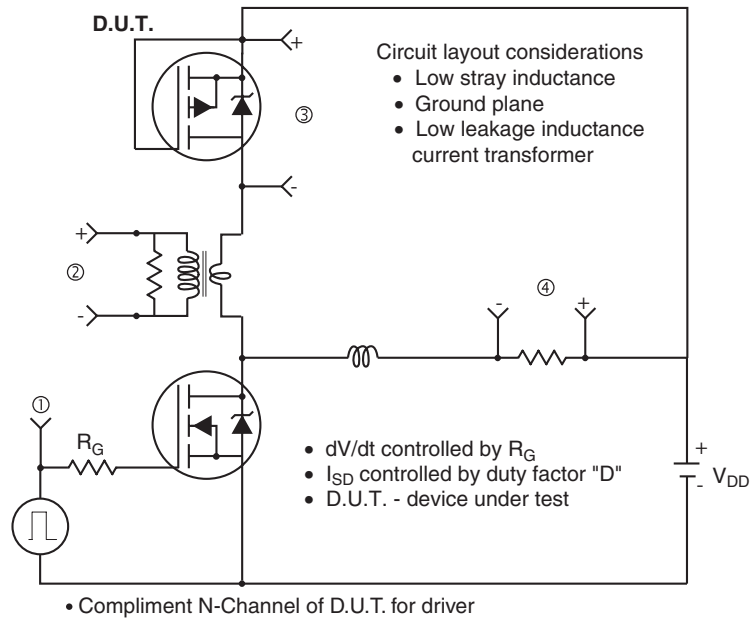


Fig. 13b - Gate Charge Test Circuit

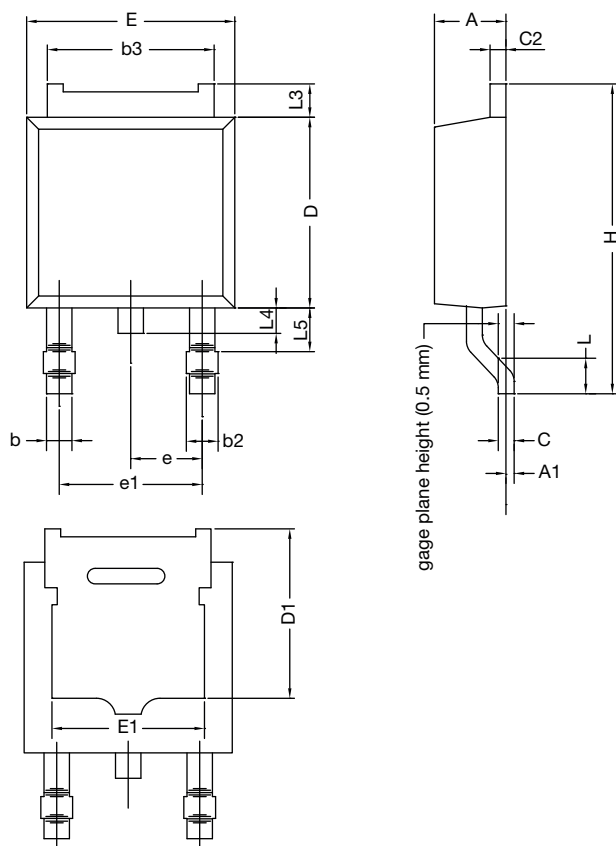
### Peak Diode Recovery $dV/dt$ Test Circuit



\*  $V_{GS} = -5 V$  for logic level and  $-3 V$  drive devices

**Fig. 14 - For P-Channel**

## TO-252AA CASE OUTLINE



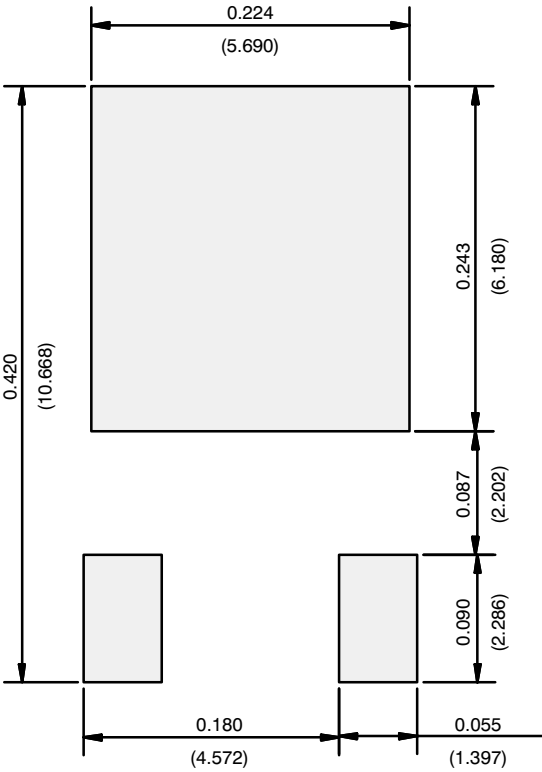
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.14	1.52	0.045	0.060
ECN: X12-0247-Rev. M, 24-Dec-12				
DWG: 5347				

### Note

- Dimension L3 is for reference only.



RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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