

## D45NF75-VB Datasheet

### N-Channel 100-V (D-S) MOSFET

#### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>a</sup>	$Q_g$ (Typ.)
100	0.0185 at $V_{GS} = 10$ V	45	38 nC

#### FEATURES

- Trench Power MOSFET
- 100 %  $R_g$  and UIS Tested

#### APPLICATIONS

- Primary Side Switch
- Isolated DC/DC Converter



**RoHS**  
COMPLIANT

TO-252



Top View



N-Channel MOSFET

#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		$V_{DS}$	100	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150$ °C)	$T_C = 25$ °C	$I_D$	45 <sup>a</sup>	A
	$T_C = 100$ °C		30	
	$T_A = 25$ °C		9.2 <sup>b</sup>	
	$T_A = 100$ °C		6.8 <sup>b</sup>	
Pulsed Drain Current		$I_{DM}$	140	
Continuous Source-Drain Diode Current	$T_C = 25$ °C	$I_S$	45 <sup>a</sup>	
	$T_A = 25$ °C		2 <sup>b</sup>	
Single Pulse Avalanche Current	$L = 0.1$ mH	$I_{AS}$	35	mJ
Avalanche Energy		$E_{AS}$	101	
Maximum Power Dissipation	$T_C = 25$ °C	$P_D$	136.4	W
	$T_C = 100$ °C		68.2	
	$T_A = 25$ °C		3 <sup>b</sup>	
	$T_A = 100$ °C		1.5 <sup>b</sup>	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to 175	°C

#### THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b</sup>	Steady State	$R_{thJA}$	40	50	°C/W
Maximum Junction-to-Case		$R_{thJC}$	0.85	1.1	

Notes:

a. Package limited.

b. Surface mounted on 1" x 1" FR4 board.

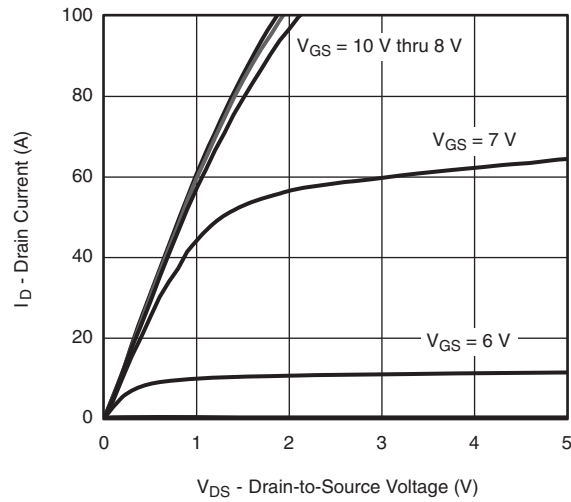
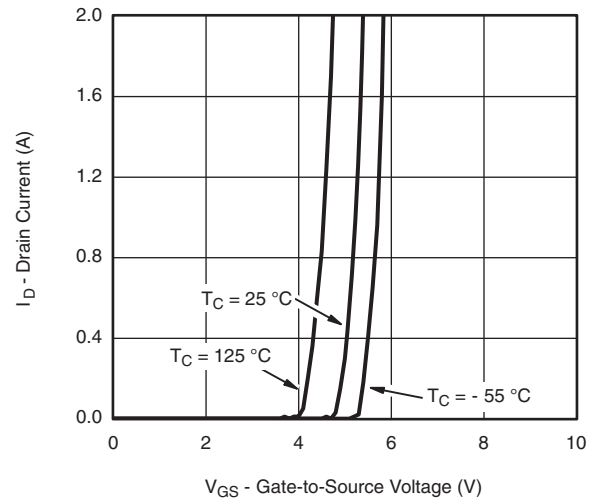
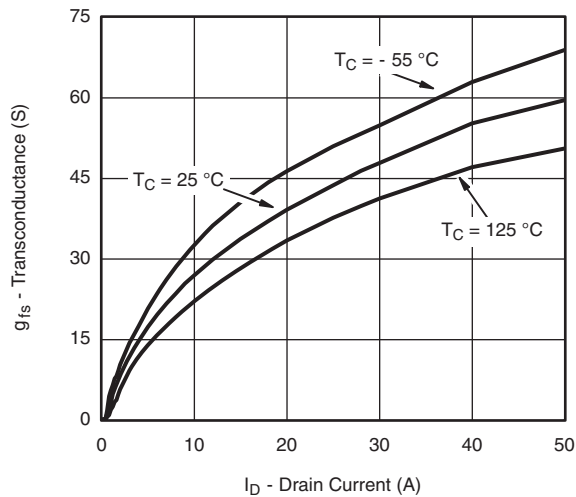
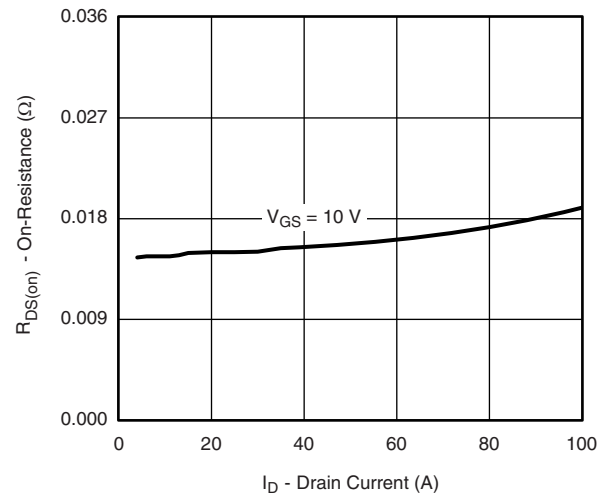
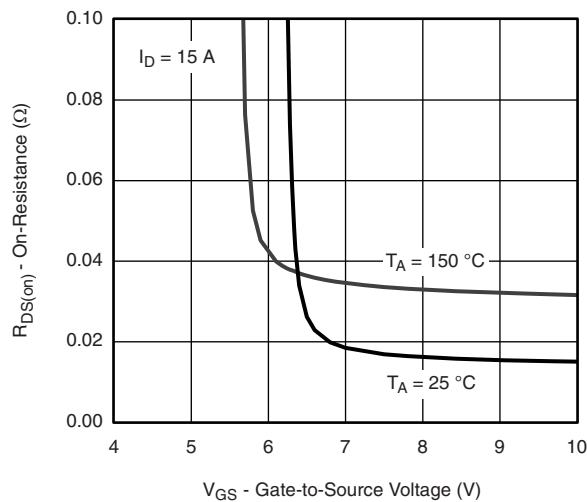
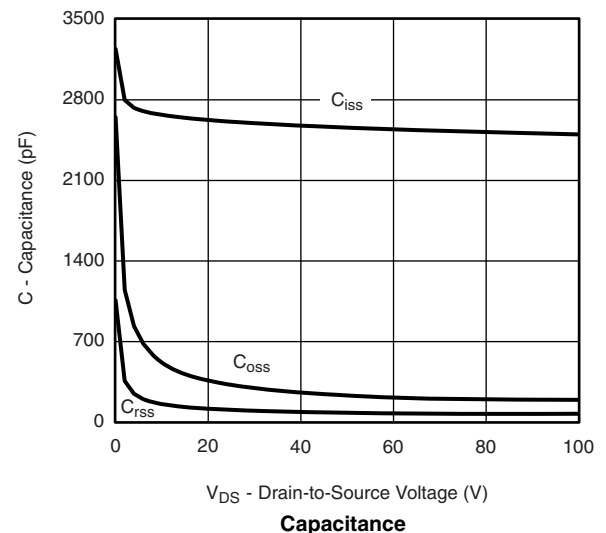
SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	100			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA		110		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			- 12.5		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.5		5	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			50	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	30			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A		0.0185		Ω
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A		33		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V, f = 1 MHz		2400		pF
Output Capacitance	C <sub>oss</sub>			230		
Reverse Transfer Capacitance	C <sub>rss</sub>			80		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 50 A		38	70	nC
Gate-Source Charge	Q <sub>gs</sub>			14		
Gate-Drain Charge	Q <sub>gd</sub>			12		
Gate Resistance	R <sub>g</sub>	f = 1 MHz		1.6	2.5	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 50 V, R <sub>L</sub> = 1 Ω I <sub>D</sub> ≅ 50 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		12	20	ns
Rise Time	t <sub>r</sub>			10	20	
Turn-Off Delay Time	t <sub>d(off)</sub>			18	35	
Fall Time	t <sub>f</sub>			8	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode	I <sub>S</sub>	T <sub>C</sub> = 25 °C			35	A
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				100	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 15 A		0.85	1.5	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 50 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C		80	120	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			160	240	nC
Reverse Recovery Fall Time	t <sub>a</sub>			57		ns
Reverse Recovery Rise Time	t <sub>b</sub>			23		

Notes:

a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise note)

**Output Characteristics**

**Transfer Characteristics**

**Transconductance**

**On-Resistance vs. Drain Current**

**On-Resistance vs. Gate-to-Source Voltage**

**Capacitance**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)


\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified  
**Safe Operating Area, Junction-to-Ambient**



\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified  
**Safe Operating Area, Junction-to-Case**



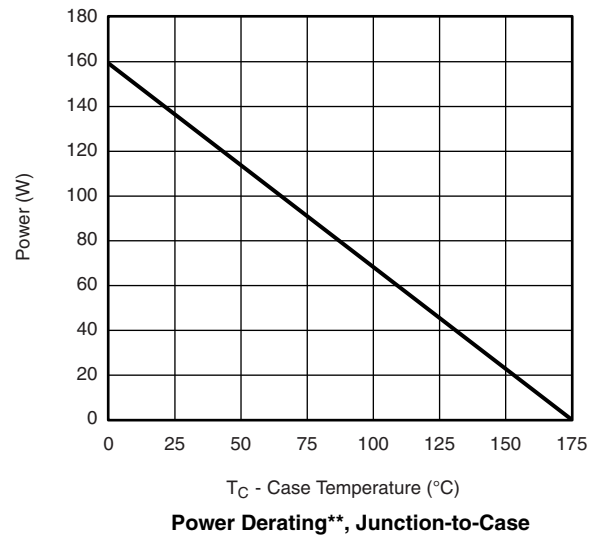
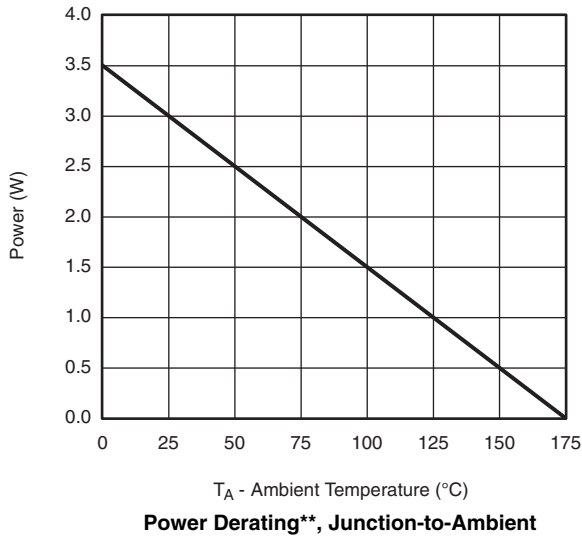
**Current Derating\*\*, Junction-to-Ambient**



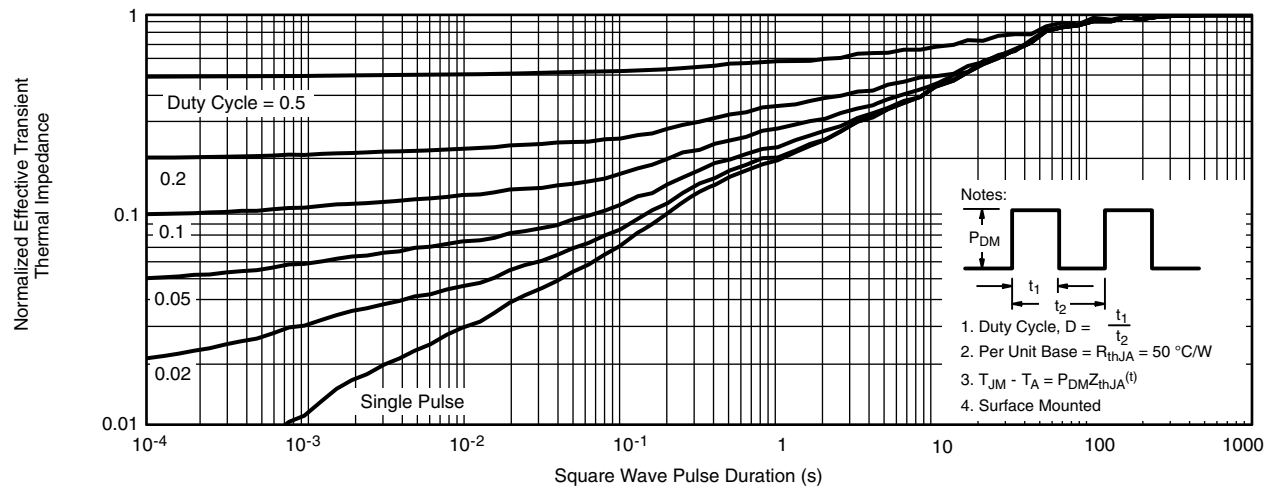
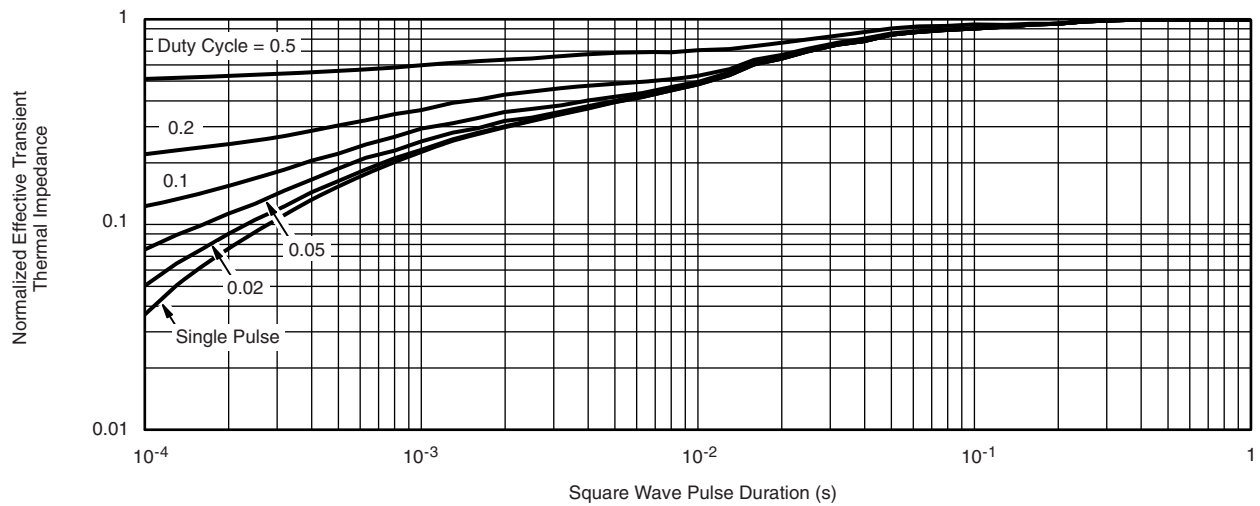
**Current Derating\*\*, Junction-to-Case**

\*\* The power dissipation  $P_D$  is based on  $T_{J(max.)} = 175^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



\*\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 175\text{ °C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Normalized Thermal Transient Impedance, Junction-to-Ambient**

**Normalized Thermal Transient Impedance, Junction-to-Case**

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