

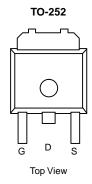
# D413-VB Datasheet P-Channel 40 V (D-S) MOSFET

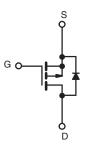
PRODUCT SUMMARY					
V <sub>DS</sub> (V)	-40				
$R_{DS(on)}(\Omega)$ at $V_{GS} = -10 \text{ V}$	0.012				
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = -4.5 \text{ V}$	0.015				
I <sub>D</sub> (A)	-50				
Configuration	Single				

## **FEATURES**

- Trench power MOSFET
- Package with low thermal resistance
- $\bullet$  100 %  $R_g$  and UIS tested







P-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>C</sub> = 25 °C, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V <sub>DS</sub>	-40	V	
Gate-Source Voltage		V <sub>GS</sub>	± 20	v	
Continuous Drain Current	$T_C = 25  ^{\circ}C^{a}$	-	-50		
	T <sub>C</sub> = 125 °C	I <sub>D</sub>	-39		
Continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	-50	Α	
Pulsed Drain Current <sup>b</sup>		I <sub>DM</sub>	-200		
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	-40		
Single Pulse Avalanche Energy	L = 0.1 MH	E <sub>AS</sub>	80	mJ	
Maximum Power Dissipation <sup>b</sup>	T <sub>A</sub> = 25 °C		3		
	T <sub>C</sub> = 25 °C	$P_{D}$	136	W	
	T <sub>C</sub> = 125 °C		45		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-Ambient	PCB Mount c	$R_{thJA}$	50	°C/W	
Junction-to-Case (Drain)		$R_{thJC}$	1.1	C/VV	

#### Notes

- a. Package limited.
- b. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.
- c. When mounted on 1" square PCB (FR4 material).
- d. Parametric verification ongoing.



PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$		-40	-	-	V	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA		-	-3.5	V	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		-	± 100	nA	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -40 V	-	-	-1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -40 V, T <sub>J</sub> = 125 °C	-	-	-50	μΑ	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = -40 V, T <sub>J</sub> = 175 °C	-	-	-150		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = -10 V	$V_{DS} \le -5 \text{ V}$	-50	-	-	Α	
		V <sub>GS</sub> = -10 V	I <sub>D</sub> = -17 A	-	0.012	-	Ω	
Daris Os association Providence		V <sub>GS</sub> = -10 V	I <sub>D</sub> = -10 A, T <sub>J</sub> = 125 °C	-	0.017	-		
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V	I <sub>D</sub> = -10 A, T <sub>J</sub> = 175 °C	-	0.020	-		
		V <sub>GS</sub> = -4.5 V	I <sub>D</sub> = -14 A	-	0.015	-		
Forward Transconductance <sup>a</sup>	9fs	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -17 A		-	61	-	S	
Dynamic <sup>b</sup>								
Input Capacitance	C <sub>iss</sub>			-	3000	-	pF	
Output Capacitance	Coss	$V_{GS} = 0 V$	V <sub>GS</sub> = 0 V V <sub>DS</sub> = -25 V, f = 1 MHz	-	508	635		
Reverse Transfer Capacitance	C <sub>rss</sub>	7		-	352	440		
Total Gate Charge <sup>c</sup>	Qg			-	60	80	nC	
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	V <sub>GS</sub> = -10 V	$V_{DS} = -30 \text{ V}, I_{D} = -50 \text{ A}$	-	5.7	8.6		
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>	7		-	14.7	22		
Gate Resistance	R <sub>g</sub>		f = 1 MHz		3	4.5	Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>				10	15		
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = -20 \text{ V}, \text{ R}_{L} = 0.4 \Omega$ $I_{D} \cong -50 \text{ A}, \text{ V}_{GEN} = -10 \text{ V}, \text{ R}_{g} = 1 \Omega$		-	12	18	ns	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	40	60		
Fall Time <sup>c</sup>	t <sub>f</sub>			-	16	24		
Source-Drain Diode Ratings and Char-	acteristics <sup>b</sup>	•						
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	-200	Α	
Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> = -50 A, V <sub>GS</sub> = 0 V		_	-1	-1.5	V	

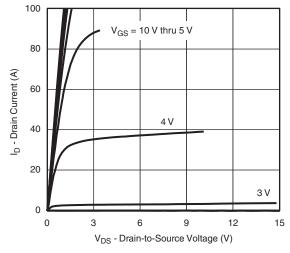
#### Notes

- a. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

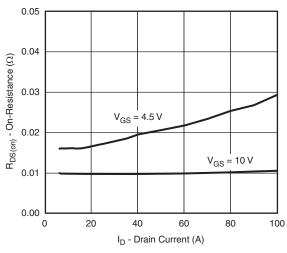
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



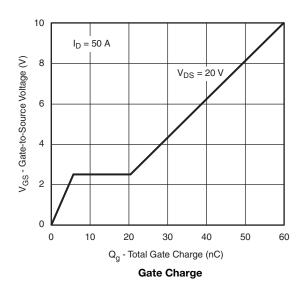
## **TYPICAL CHARACTERISTICS** ( $T_A = 25$ °C, unless otherwise noted)

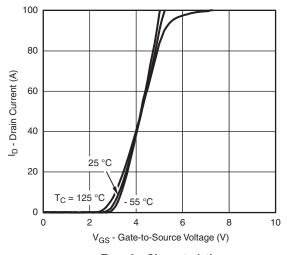


## **Output Characteristics**

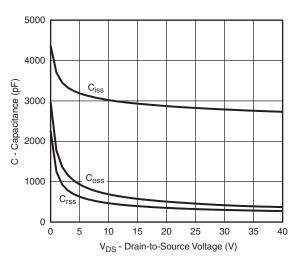


On-Resistance vs. Drain Current

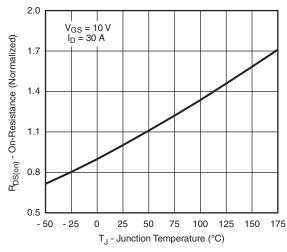




**Transfer Characteristics** 



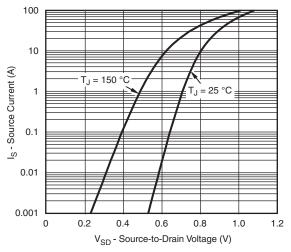
Capacitance

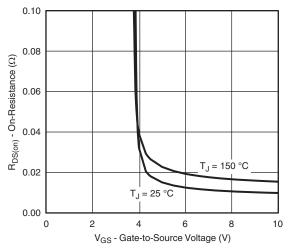


On-Resistance vs. Junction Temperature



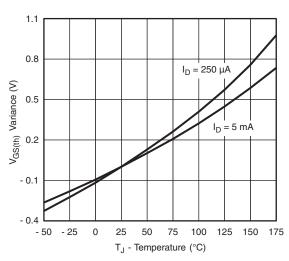
## TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)

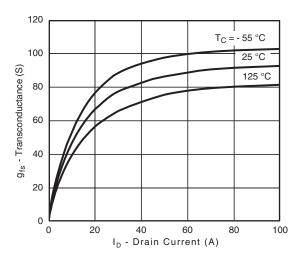




### **Source Drain Diode Forward Voltage**

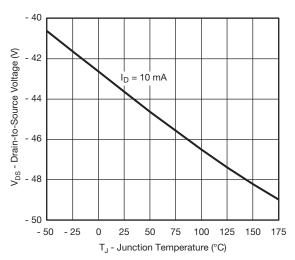






## **Threshold Voltage**

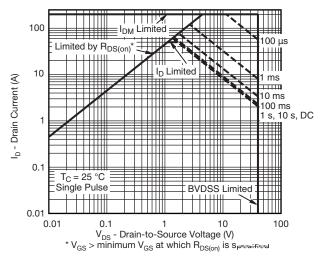
Transconductance



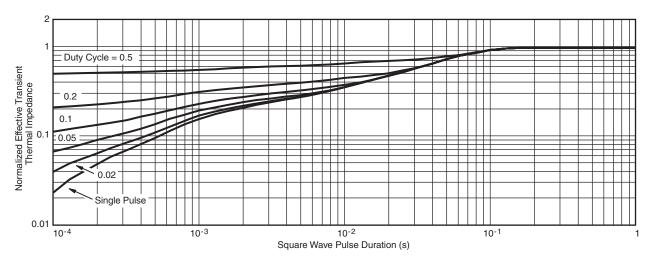
**Drain Source Breakdown vs. Junction Temperature** 



## **TYPICAL CHARACTERISTICS** ( $T_A = 25$ °C, unless otherwise noted)



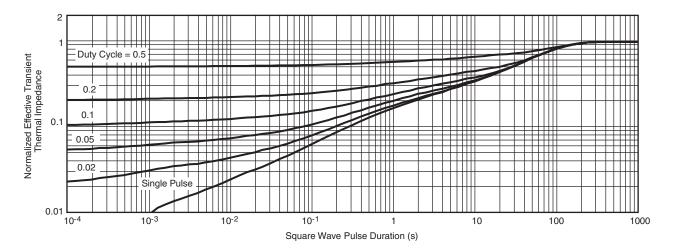
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

服务热线:400-655-8788 5





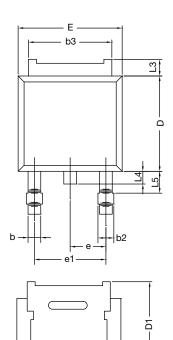
### Normalized Thermal Transient Impedance, Junction-to-Ambient

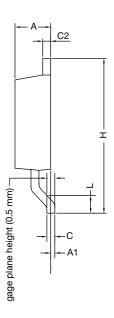
#### Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.



## **TO-252AA Case Outline**





	MILLIN	METERS	INCHES		
DIM.	MIN.	MAX.	MIN.	MAX.	
Α	2.18	2.38	0.086	0.094	
A1	-	0.127	-	0.005	
b	0.64	0.88	0.025	0.035	
b2	0.76	1.14	0.030	0.045	
b3	4.95	5.46	0.195	0.215	
С	0.46	0.61	0.018	0.024	
C2	0.46	0.89	0.018	0.035	
D	5.97	6.22	0.235	0.245	
D1	4.10	-	0.161	-	
E	6.35	6.73	0.250	0.265	
E1	4.32	-	0.170	-	
Н	9.40	10.41	0.370	0.410	
е	2.28	BSC	0.090 BSC		
e1	4.56 BSC		0.180 BSC		
L	1.40	1.78	0.055	0.070	
L3	0.89	1.27	0.035	0.050	
L4	-	1.02	-	0.040	
L5	1.01	1.52	0.040	0.060	
ECN: T13-0592-Rev. A, 02-Sep-13					

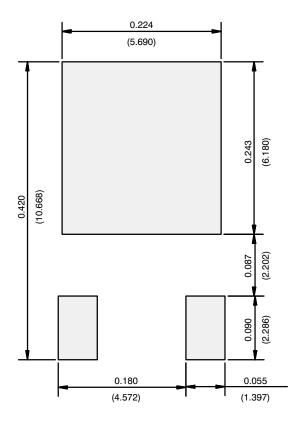
DWG: 6019

## Note

• Dimension L3 is for reference only.



## **RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)**



Recommended Minimum Pads Dimensions in Inches/(mm)



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